STIC EIC 2100
Search Request Form

Today's Date: 5/5/03

What date would you like to use to limit the search?
Priority Date: Other:

Name Ayal Shavon
AU 2123 Examiner # 2123
Room # 5D53 Phone 306-0297
Serial # _____

Format for Search Results (Circle One):
PAPER DISK EMAIL
Where have you searched so far?
USP DWPI EPO JPO ACM IBM TDB
IEEE INSPEC SPI Other _____

Is this a "Fast & Focused" Search Request? (Circle One) (YES) NO
A "Fast & Focused" Search is completed in 2-3 hours (maximum). The search must be on a very specific topic and meet certain criteria. The criteria are posted in EIC2100 and on the EIC2100 NPL Web Page at http://ptoweb/patents/stic/stic-tc2100.htm.

What is the topic, novelty, motivation, utility, or other specific details defining the desired focus of this search? Please include the concepts, synonyms, keywords, acronyms, definitions, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract, background, brief summary, pertinent claims and any citations of relevant art you have found.

Database for storing VHDL code, documentation, and translation of VHDL code to an FPGA-specific format.

[Example: DC2NCF is used to translate VHDL to a format that can be read by XACT MI - a tool made by Xilinx.]

The database is connected to debuggers and editors.
The document can be in the form of comments embedded into the code.

STIC Searcher David Holloway Phone 308-7794
Date picked up 5-5-03 Date Completed 5-6-03

Time 99 minutes

Search and Information Resources Administration

Databases - DIALOG, Inspec, Compendex & Google

Examiner Sharon:
Attached please find the results of your search request re:
VHDL & FPGAs

Please let me know if you would like to try a refocused search with additional terms or strategies.

David Holloway
308-7794

```
Set     Items   Description
S1    1211580   ASIC OR FPGA OR PROGRAMMABLE()GATE()ARRAY OR PLC OR PLD OR
            PROGRAMMABLE()LOGIC()(DEVICE? OR CONTROL?)
S2      20249   VHDL OR VERY()HIGH()SPEED()INTEGRATED()CIRCUIT()DESCRIPTION
S3    4791297   CONVERT? OR CONVERS? OR TRANSLAT? OR TRANSFORM? OR COMPIL?
S4          0   DC2NCF AND S2
S5        367   S1(10N)S2(3N)S3
S6        211   RD (unique items)
S7        181   S6 AND (DEBUG? OR EMULAT? OR MODEL? OR SIMULAT?)
S8          7   S6 (S)(DATABASE? OR DATABANK? OR DB OR RDB OR RDBMS OR DBMS
              OR OODB?)
S9         95   S6(S)(DEBUG? OR EMULAT? OR MODEL  OR SIMULAT?)
S10        99   S8 OR S9
S11        98   RD (unique items)
S12        10   S9 AND (DB OR DATABASE? OR DATABANK? OR DATAFILE? OR RDBS -
              OR DBMS)
S13        14   S8 OR S12
S14        14   RD (unique items)
File 275:Gale Group Computer DB(TM) 1983-2003/May 05
         (c) 2003 The Gale Group
File  47:Gale Group Magazine DB(TM) 1959-2003/May 02
         (c) 2003 The Gale group
File 636:Gale Group Newsletter DB(TM) 1987-2003/May 05
         (c) 2003 The Gale Group
File  16:Gale Group PROMT(R) 1990-2003/May 05
         (c) 2003 The Gale Group
File 624:McGraw-Hill Publications 1985-2003/May 05
         (c) 2003 McGraw-Hill Co. Inc
File 484:Periodical Abs Plustext 1986-2003/Apr W4
         (c) 2003 ProQuest
File 613:PR Newswire 1999-2003/May 06
         (c) 2003 PR Newswire Association Inc
File 813:PR Newswire 1987-1999/Apr 30
         (c) 1999 PR Newswire Association Inc
File 141:Readers Guide 1983-2003/Mar
         (c) 2003 The HW Wilson Co
File 239:Mathsci 1940-2003/Jun
         (c) 2003 American Mathematical Society
File 696:DIALOG Telecom. Newsletters 1995-2003/May 05
         (c) 2003 The Dialog Corp.
File 621:Gale Group New Prod.Annou.(R) 1985-2003/May 05
         (c) 2003 The Gale Group
File 674:Computer News Fulltext 1989-2003/Apr W4
         (c) 2003 IDG Communications
File 369:New Scientist 1994-2003/Apr W3
         (c) 2003 Reed Business Information Ltd.
File 160:Gale Group PROMT(R) 1972-1989
         (c) 1999 The Gale Group
File 635:Business Dateline(R) 1985-2003/May 03
         (c) 2003 ProQuest Info&Learning
File  15:ABI/Inform(R) 1971-2003/May 03
         (c) 2003 ProQuest Info&Learning
File   9:Business & Industry(R) Jul/1994-2003/May 05
         (c) 2003 Resp. DB Svcs.
File  13:BAMP 2003/Apr W4
         (c) 2003 Resp. DB Svcs.
File 810:Business Wire 1986-1999/Feb 28
         (c) 1999 Business Wire
File 610:Business Wire 1999-2003/May 06
         (c) 2003 Business Wire.
File 647:CMP  Computer Fulltext 1988-2003/Apr W2
         (c) 2003 CMP Media, LLC
File  98:General Sci Abs/Full-Text 1984-2003/Mar
         (c) 2003 The HW Wilson Co.
File 148:Gale Group Trade & Industry DB 1976-2003/May 05
         (c)2003 The Gale Group
```

14/3,K/1 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2003 The Gale Group. All rts. reserv.

02160513 SUPPLIER NUMBER: 20444218 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Memec has global designs. (Memec Design Services) (Company Business and Marketing)
Steffora, Ann
Electronic News (1991), v44, n2211, p44(1)
March 23, 1998
ISSN: 1061-6624 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 659 LINE COUNT: 00056

... these designs, which can bring new life to an end-of-life design. MDS performs **VHDL** or Verilog **database** transcriptions, **converting** older schematic and HDL designs to current **FPGA** design tools that enable the customer to modify or build logic around the design. MDS...

14/3,K/2 (Item 2 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2003 The Gale Group. All rts. reserv.

01538349 SUPPLIER NUMBER: 12776049 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Chips: TriQuint adopts Mentor Graphics' top-down tool suite; Mentor Graphics & leading gallium arsenide IC supplier partner for next-generation GaAs design. (TriQuint Semiconductor Inc.; integrated circuit)
EDGE, on & about AT&T, v7, n220, p15(1)
Oct 12, 1992
LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 523 LINE COUNT: 00043

... AutoLogic for synthesis; FlexTest for automatic test vector generation; QuickSim II for mixed-level logic **simulation** ; the System-1076 **VHDL compiler** ; CheckMate for IC verification; and QuickPlan, a newly announced **ASIC** floor planning tool jointly developed by Texas Instruments and Mentor Graphics.
In addition to supplying...

...and ASIC development that takes us from design creation through automated test with a common **database** of models. The resulting benefits in design predictability and validation will give TriQuint and its...

14/3,K/3 (Item 3 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2003 The Gale Group. All rts. reserv.

01463817 SUPPLIER NUMBER: 11633454 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Retargeting in a mixed top-down/bottom-up design methodology. (circuit design methodologies)
Mattison, Roland
Computer Design, v30, n15, p81(1)
Dec, 1991
ISSN: 0010-4566 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 1069 LINE COUNT: 00084

... or parameterized parts can also be instantiated directly in the schematic.
Abel or existing JEDEC **PLD** designs can be **converted** into full timing- **simulatable** and synthesizable **VHDL** using new alternate forms of entry (AFE) tools. A VHDL system **simulator** can be used to verify the design at this point in the design process, mixing...

...descriptions. VHDL modules can be inserted into the design to create the stimulus for the **simulation** using high-level language capabilities.
The logic designer can then use synthesis applications supporting

behavioral...
...toolkits for many CAE systems which take the final optimized design out of the design **database** and convert it into its required format. Tools are also available to base-annotate the...

14/3,K/4 (Item 4 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2003 The Gale Group. All rts. reserv.

01310325 SUPPLIER NUMBER: 07689148 (USE FORMAT 7 OR 9 FOR FULL TEXT)
VHDL and tool integration star at 26th DAC. (Design Automation Conference)
Phillips, Barry
ESD: The Electronic System Design Magazine, v19, n8, p19(2)
August, 1989
ISSN: 0893-2565 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 1126 LINE COUNT: 00096

... the availability of VHDL models has been limited, this is changing as mixed-mode behavioral **VHDL simulation** becomes viable. In 1988, Vantage developed a **VHDL translator** for **ASIC simulation** models on National Semiconductor's DY-4 platform. Since then, Vantage has contracted with Logic...unrestricted basis. Access to the Mentor Graphics' human interface, or read/write access to internal **databases** requires negotiation (typically involving royalty payments). Nondisclosure agreements protect the terms of the OpenDoor relationship...

14/3,K/5 (Item 1 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2003 The Gale Group. All rts. reserv.

06324720 Supplier Number: 54584193 (USE FORMAT 7 FOR FULLTEXT)
FPGA designers move on to the Web.
Electronics Times, pII
May 4, 1999
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 2154

... actually good for the designer?
The idea that the software is maintained on a central **database** and designs are sent in text as **VHDL** or Verilog to be **compiled** remotely is appealing to the **FPGA** companies, as it would dramatically reduce the issues of software support. But there are some...

14/3,K/6 (Item 2 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2003 The Gale Group. All rts. reserv.

05523591 Supplier Number: 48372061 (USE FORMAT 7 FOR FULLTEXT)
Memec Has Global Designs
Electronic News (1991), p44
March 23, 1998
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 638

... these designs, which can bring new life to an end-of-life design. MDS performs **VHDL** or Verilog **database** transcriptions, **converting** older schematic and HDL designs to current **FPGA** design tools that enable the customer to modify or build logic around the design. MDS...

14/3,K/7 (Item 3 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2003 The Gale Group. All rts. reserv.

05044938 Supplier Number: 47405658 (USE FORMAT 7 FOR FULLTEXT)
New LASAR-VT Option Enables Use of VHDL/VITAL Models for Digital Min/Max Simulation
PR Newswire, p0522NETH021
May 22, 1997
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 934

... Models Speeds Test Development
The new LASAR-VT option provides a simple, automated process for **converting** **ASIC** and **FPGA** macrocells and device models expressed in **VHDL** 's VITAL language from design **databases** into LASAR test **simulation** models. These models support all the features required for high-fault-coverage digital test program development and diagnostics: min/max timing and fault **simulation** , and backannotation of post-layout timing information expressed in Standard Delay Format (SDF), OVI 2...

...process that eliminates the need for development and maintenance of separate design and test model **databases** ."
Noted Rolince, "Model development, by itself, can account for up to 40% of the time...

14/3,K/8 (Item 4 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2003 The Gale Group. All rts. reserv.

02891364 Supplier Number: 43901104 (USE FORMAT 7 FOR FULLTEXT)
VHDL looks for open ASIC library
Electronic Engineering Times, p70
June 14, 1993
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 1363

... No standard exists for handling back-annotation of timing data from layout. As a result, **ASIC** vendors have been forced to create specialized **translation** tools targeted to each proprietary **simulator** .
VHDL holds the promise of providing a standard language that solves many of these problems...VML descriptions by hand, an easy approach would be to translate from existing ASIC-vendor **databases** to VML automatically. Once the VML is available, a compiler creates an intermediate **database** format. A programmatic interface is available that gives third parties an open interface for easy...

14/3,K/9 (Item 5 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2003 The Gale Group. All rts. reserv.

02687439 Supplier Number: 43587183 (USE FORMAT 7 FOR FULLTEXT)
Isdata plans Windows PLD tool
Electronic Engineering Times, p46
Jan 18, 1993
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 377

... This package, to be available in March from Isdata's Oakland, Calif., office, includes a **PLD** **compiler** , partitioner and **database** . Windows support for Isdata's **VHDL** and functional-verification capabilities will be added later this year. Users can exchange a current...

14/3,K/10 (Item 6 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

(c) 2003 The Gale Group. All rts. reserv.

02051026 Supplier Number: 42648901 (USE FORMAT 7 FOR FULLTEXT)
VHDL's missing link: the gate level: USERS LOOK FOR OTHER TOOLS TO COMPLETE DESIGNS
Electronic Engineering Times, p27
Jan 6, 1992
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 2447

... got the QuickSim environment, and we have a lot of tools that run off that **database** , like static timing analysis," he added. "So it made more sense to go directly to...Mendes da Costa of Mentor acknowledged that if System 1076 users turn to the non- **VHDL** QuickSim **ASIC** libraries, they aren't really staying in the **VHDL** environment. But they avoid the net-list and test-vector **translations** that would be required in moving to a different **simulator** .

Harris's Bohm believes incomplete VHDL support is not a fair trade-off for access...

14/3,K/11 (Item 1 from file: 813)
DIALOG(R)File 813:PR Newswire
(c) 1999 PR Newswire Association Inc. All rts. reserv.

1102385 NETH021
LASAR V6.52 Upgrade Features Ease-of-Use Enhancements

DATE: May 22, 1997 12:11 EDT WORD COUNT: 913

...Models Speeds Test Development

The new LASAR-VT option provides a simple, automated process for **converting** **ASIC** and **FPGA** macrocells and device models expressed in **VHDL** 's VITAL language from design **databases** into LASAR test **simulation** models. These models support all the features required for high-fault-coverage digital test program development and diagnostics: min/max timing and fault **simulation** , and backannotation of post-layout timing information expressed in Standard Delay Format (SDF), OVI 2...

... process that eliminates the need for development and maintenance of separate design and test model **databases** ."

Noted Rolince, "Model development, by itself, can account for up to 40% of the time...

14/3,K/12 (Item 1 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)
(c) 2003 ProQuest Info&Learning. All rts. reserv.

02134636 69619043
The perfect systems design strategy
Newcomb, Jesse
Printed Circuit Design v18n3 PP: 10-13 Mar 2001
JRNL CODE: PCC
WORD COUNT: 2538

...TEXT: view of the complete system. Because the new tools were based on a unified hierarchical **database** instead of sheet drawings, they provided our staff with a modular framework. When properly laid...long lead times, such as custom high-density connectors and power supply magnetics.

When the **ASIC** designers began to **translate** the early C code into **VHDL** , explicit port assignments were made at the pad ring level. The VHDL pad ring files...

... editor. These early pad[redacted]ng assignments were then used t[redacted] create VHDL netlists for interASIC **simulation** .

But the initial import was not the key step. Since ASIC port assignments were constantly...Having completely closed the schematic-to-layout loop, we could freely autoroute and update the **databases** from either side.

Standards certification as a long-load task

Since no products could be...

14/3,K/13 (Item 1 from file: 810)
DIALOG(R)File 810:Business Wire
(c) 1999 Business Wire . All rts. reserv.

0299520 BW135

MENTOR GRAPHICS TRIQUINT: TRIQUINT ADOPTS MENTOR GRAPHICS' TOP-DOWN TOOL SUITE; Mentor Graphics and leading gallium arsenide IC supplier partner for next-generation GaAs design

October 6, 1992

Byline: Business Editors

...AutoLogic for synthesis; FlexTest for automatic test vector generation; QuickSim II for mixed-level logic **simulation** ; the System-1076 **VHDL compiler** ; CheckMate for IC verification; and QuickPlan, a newly announced ASIC floor planning tool jointly developed...

...and ASIC development that takes us from design creation through automated test with a common **database** of models. The resulting benefits in design predictability and validation will give TriQuint and its...

14/3,K/14 (Item 1 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2003 The Gale Group. All rts. reserv.

06223328 SUPPLIER NUMBER: 14330544 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Tool set joins synthesis with simulation for reliable ASIC design. (application specific integrated circuit) (Mentor Graphics Corp.'s Top Down Design-Solver) (Product Announcement)
Napier, John C.
EDN, v37, n24, p72(1)
Nov 26, 1992
DOCUMENT TYPE: Product Announcement ISSN: 0012-7515 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 450 LINE COUNT: 00036

...ABSTRACT: RTL), HDL, and a design's gate-level descriptions. A single application specific integrated circuit (**ASIC**) library is used by the software, along with a **VHDL compiler** , a timing calculator, a common tool **database** and a **simulator** .
... data and functions wherever possible and have consistent timing models. The software uses a single **ASIC** library, one timing calculator, one **VHDL** (VHSIC-hardware-description-language) **compiler** for both synthesis and **simulation** , one **simulator** for both behavioral and gate-level work, and a common **database** for all tools.
Five ASIC and FPGA (field-programmable-gate-array) vendors (Fujitsu,

```
Set     Items   Description
S1      48820   ASIC OR FPGA OR PROGRAMMABLE()GATE()ARRAY OR PLC OR PLD OR
             PROGRAMMABLE()LOGIC()(DEVICE? OR CONTROL?)
S2        606   VHDL OR VERY()HIGH()SPEED()INTEGRATED()CIRCUIT()DESCRIPTION
S3     771717   CONVERT? OR CONVERS? OR TRANSLAT? OR TRANSFORM? OR COMPIL?
S4          0   DC2NCF AND S2
S5        268   S1 AND S2 AND S3
S6        303   S1 AND S2
S7        128   S1(S)S2
S8         37   S7(S)S3
S9         27   S8 AND IC=(G06F? OR H04L?)
S10        27   IDPAT (sorted in duplicate/non-duplicate order)
S11        27   IDPAT (primary/non-duplicate records only)
File 348:EUROPEAN PATENTS 1978-2003/Apr W04
         (c) 2003 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20030501,UT=20030424
         (c) 2003 WIPO/Univentio
```

11/5/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2003 European Patent Office. All rts. reserv.

01444845
Embedded logic analyser
Eingebetteter logischer Analysator
Analyseur logique integre
PATENT ASSIGNEE:
Altera Corporation, (398574), 101 Innovation Drive, San Jose, California 95134, (US), (Applicant designated States: all)
INVENTOR:
Veenstra, Kerry, 1906 Conifer Court, San Jose, California 95132, (US)
Rangasayee,Krishna, 2350 Meadowlake Drive, Pleasanton, CA 94566, (US)
Herrmann, Alan L., 727 Winstead Terrace, Sunnyvale, California 94087, (US)
LEGAL REPRESENTATIVE:
O'Connell, David Christopher (62551), Haseltine Lake & Co., Imperial House, 15-19 Kingsway, London WC2B 6UD, (GB)
PATENT (CC, No, Kind, Date): EP 1233341 A1 020821 (Basic)
APPLICATION (CC, No, Date): EP 2002009367 981118;
PRIORITY (CC, No, Date): US 65602 P 971118; US 186607 981106
DESIGNATED STATES: DE; FR; GB; IT; NL
RELATED PARENT NUMBER(S) - PN (AN):
EP 919916 (EP 98309432)
INTERNATIONAL PATENT CLASS: **G06F-011/25** ; G01R-031/3177; G01R-031/3185

ABSTRACT EP 1233341 A1
Embedding a logic analyzer in a programmable logic device allows signals to be captured both before and after a trigger condition (breakpoint). A logic analyzer embedded within a PLD captures and stores logic signals. It unloads these signals for viewing on a computer. Using an electronic design automation (EDA) software tool running on a computer system, an engineer specifies signals of the PLD to be monitored, a breakpoint, total number of samples to be stored, number of samples to be captured after the breakpoint occurs, and a system clock signal. The EDA tool automatically inserts the logic analyzer into the electronic design of the PLD which is compiled and downloaded to configure the PLD. Using an interface connected between the PLD and the computer, the EDA tool commands the embedded logic analyzer to run. Signals are stored continuously while running in a ring buffer RAM memory. Once the breakpoint occurs, more samples are captured if desired, in addition to those signals captured before breakpoint. The EDA tool directs the logic analyzer to unload the data from its capture buffer for display on a computer. The breakpoint and sample number can be changed without recompiling. A JTAG port controls the logic analyzer. Inputs and outputs of the logic analyzer are routed to unbonded JTAG-enabled I/O cells. Alternatively, a user-implemented test data register provides a JTAG-like chain of logic elements through which control and output information is shifted. Stimulus cells provide control information to the logic analyzer, and sense cells retrieve data from the logic analyzer.
ABSTRACT WORD COUNT: 255
NOTE:
Figure number on first page: 5

LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 020821 A1 Published application with search report
Change: 030102 A1 Inventor information changed: 20021108
Examination: 030319 A1 Date of request for examination: 20030115
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200234	682
SPEC A	(English)	200234	17651
Total word count - document A			18333
Total word count - document B			0
Total word count - documents A + B			18333

11/5/2 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2003 European Patent Office. All rts. reserv.

01371685
Virtual hardware machine methods and devices
Verfahren und Gerate fur virtuelle Hardware-Maschine
Procedes et appareils pour des machines hardware virtuelles
PATENT ASSIGNEE:
INTERUNIVERSITAIRE MICROELEKTRONICA CENTRUM VZW, (1021501), Kapeldreef 75 , 3001 Leuven, (BE), (Applicant designated States: all)
INVENTOR:
Ha, Yajun, 95 Chen Lan Road, Changsha, CH-Hunen 410002, P.R., (CN)
Schaumont, Patrick, Nieuwstraat 16, B-3018 Wijgmaal, (BE)
Engels, Marc, Rotselaarsesteenweg 118, B-3018 Wijgmaal, (BE)
Vernalde, Serge, Kapucijnenvoer 114A/401, B-3000 Leuven, (BE)
LEGAL REPRESENTATIVE:
Bird, William Edward et al (62355), Bird Goen & Co., Vilvoordsebaan 92, 3020 Winksele, (BE)
PATENT (CC, No, Kind, Date): EP 1168168 A2 020102 (Basic)
APPLICATION (CC, No, Date): EP 2001202357 010620;
PRIORITY (CC, No, Date): US 212906 P 000620
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE; TR
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: **G06F-009/46**

ABSTRACT EP 1168168 A2
The invention relates to methods and apparatus suitable for executing a service or application at a client peer or client side, having a client specific device or client specific platform with a reconfigurable architecture, said service or application being provided from a service peer or a service side. A substantial part of the design effort at the service peer is re-usable at the client side.
An overall method is provided for executing an application at at least one client peer having a client specific device, the application being provided from a service peer is disclosed wherein a first code, e.g. an abstract bytecode, determined at said service peer by performing a compilation of said application on a virtual device which is at least partly reconfigurable and is representative for a set or class of devices, is transmitted from said service peer to at least said client peer. Within said method said second code is transformed at said client peer into a second code, e.g. a native bytecode, for said client specific device which is part of said class of devices and being at least partly reconfigurable by exploiting said second code.
ABSTRACT WORD COUNT: 192
NOTE:
Figure number on first page: 2

LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 020102 A2 Published application without search report
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200201	968
SPEC A	(English)	200201	6506
Total word count - document A			7474
Total word count - document B			0
Total word count - documents A + B			7474

11/5/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2003 European Patent Office. All rts. reserv.

01313555

LUCENT TECHNOLOGIES INC., (243720), 600 Mountain Avenue, Murray Hill, New Jersey 07974-0636, (US), (Applicant designated States: all)
INVENTOR:
Johnson, Robert Everest, 161 Reservoir Avenue, Morris, New Jersey 07869, (US)
LEGAL REPRESENTATIVE:
Buckley, Christopher Simon Thirsk et al (28911), Lucent Technologies Inc.,5 Mornington Road, Woodford Green, Essex IG8 0TU, (GB)
PATENT (CC, No, Kind, Date): EP 997809 A2 000503 (Basic)
APPLICATION (CC, No, Date): EP 99308204 991018;
PRIORITY (CC, No, Date): US 181815 981029
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: **G06F-001/03**
ABSTRACT EP 997809 A2

A digital synthesizer (18) includes a memory (12) containing values representing amplitudes of a signal such as a sinewave, a digital/analog converter (14) for converting outputs from the memory into an analog signal, and a counter (10) for counting by a predetermined fixed increment, which operates at a high frequency to enable the generation of very precise frequency waveforms. The digital synthesizer has many practical applications including the generation of precise signals to extract information from input radio frequency signals, the obtaining of a precise frequency from a low-cost clock, and the use as a component of a FSK modulator to permit selection between signals of multiple frequencies without any phase discontinuity. Finally, the digital synthesizer can be used in combination with an 8-bit memory, to generate a 10-bit input to a digital-to-analog converter.

ABSTRACT WORD COUNT: 135
NOTE:
Figure number on first page: 2

LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 000503 A2 Published application without search report
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200018	416
SPEC A	(English)	200018	4000
Total word count - document A			4416
Total word count - document B			0
Total word count - documents A + B			4416

11/5/5 (Item 5 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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01034790
Embedded logic analyzer
Eingebetter Logikanalysator
Analyseur logique imbrique
PATENT ASSIGNEE:
Altera Corporation, (398574), 101 Innovation Drive, San Jose, California 95134, (US), (Applicant designated States: all)
INVENTOR:
Veenstra, Kerry, 1906 Conifer Court, San Jose, California 95132, (US)
Rangasayee, Krishna, 1291 Vincente Drive, #242, Sunnyvale, California 94086, (US)
Herrmann, Alan L., 727 Winstead Terrace, Sunnyvale, california 94087, (US)
LEGAL REPRESENTATIVE:
O'Connell, David Christopher et al (62551), Haseltine Lake & Co., Imperial House, 15-19 Kingsway, London WC2B 6UD, (GB)
PATENT (CC, No, Kind, Date): EP 919916 A2 990602 (Basic)
EP 919916 A3 000112
APPLICATION (CC, No, Date): EP 98309432 981118;

PRIORITY (CC, No, Date): US [redacted]02 P 971118; US 186607 P 98110[redacted]
DESIGNATED STATES: DE; FR; GB; IT; NL
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
RELATED DIVISIONAL NUMBER(S) - PN (AN):
(EP 2002009367)
INTERNATIONAL PATENT CLASS: **G06F-011/25** ; G01R-031/3177; G01R-031/3185

ABSTRACT EP 919916 A2
Embedding a logic analyzer in a programmable logic device allows signals to be captured both before and after a trigger condition (breakpoint). A logic analyzer embedded within a PLD captures and stores logic signals. It unloads these signals for viewing on a computer. Using an electronic design automation (EDA) software tool running on a computer system, an engineer specifies signals of the PLD to be monitored, a breakpoint, total number of samples to be stored, number of samples to be captured after the breakpoint occurs, and a system clock signal. The EDA tool automatically inserts the logic analyzer into the electronic design of the PLD which is compiled and downloaded to configure the PLD. Using an interface connected between the PLD and the computer, the EDA tool commands the embedded logic analyzer to run. Signals are stored continuously while running in a ring buffer RAM memory. Once the breakpoint occurs, more samples are captured if desired, in addition to those signals captured before breakpoint. The EDA tool directs the logic analyzer to unload the data from its capture buffer for display on a computer. The breakpoint and sample number can be changed without recompiling. A JTAG port controls the logic analyzer. Inputs and outputs of the logic analyzer are routed to unbonded JTAG-enabled I/O cells. Alternatively, a userimplemented test data register provides a JTAG-like chain of logic elements through which control and output information is shifted. Stimulus cells provide control information to the logic analyzer, and sense cells retrieve data from the logic analyzer.
ABSTRACT WORD COUNT: 255
NOTE:
Figure number on first page: 5

LEGAL STATUS (Type, Pub Date, Kind, Text):

Examination:	000906 A2	Date of request for examination: 20000710
Change:	20000112 A2	International Patent Classification changed: 19991123
Change:	020626 A2	Application number of divisional application (Article 76) changed: 20020507
Examination:	020130 A2	Date of dispatch of the first examination report: 20011213
Application:	990602 A2	Published application (A1with Search Report ;A2without Search Report)
Search Report:	20000112 A3	Separate publication of the search report

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9922	1737
SPEC A	(English)	9922	17654
Total word count - document A			19391
Total word count - document B			0
Total word count - documents A + B			19391

11/5/6 (Item 6 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00987065 **Image available**
RECONFIGURABLE MEASUREMENT SYSTEM UTILIZING A PROGRAMMABLE HARDWARE ELEMENT AND FIXED HARDWARE RESOURCES
SYSTEME DE MESURE RECONFIGURABLE UTILISANT UN ELEMENT MATERIEL ET DES RESSOURCES MATERIELLES FIXES
Patent Applicant/Assignee:
NATIONAL INSTRUMENTS CORPORATION, 11500 North MoPac Expressway, Building B, Austin, TX 78759, US, US (Residence), US (Nationality)

Inventor(s):
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BUTLER Cary Paul, 6333 Yaupon Drive, Austin, TX 78759, US,
TRUCHARD James J, 3816 Hunterwood PT, Austin, TX 78746, US,
PETERSON Newton G, 1729 Cricket Hollow, Austin, TX 78758, US,
NOVACEK Matthew, 3201 Century Park Boulevard, #821, Austin, TX 78727, US,

Legal Representative:
CONLEY ROSE & TAYON P C (agent), HOOD, Jeffrey, C., P.O. Box 398, Austin, TX 78767-0398, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200317149 A2 20030227 (WO 0317149)
Application: WO 2002US22895 20020718 (PCT/WO US0222895)
Priority Application: US 2001312252 20010814; US 2001313136 20010817; US 200158150 20011029
Designated States: JP
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
Main International Patent Class: **G06F-017/50**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 44081

English Abstract
A system and method for configuring a device to perform a function, where the device includes a programmable hardware element and one or more fixed hardware resources. A program is stored which represents the function. A hardware configuration program is generated based on the program, specifying a configuration for the programmable hardware element that implements the function, and usage of the fixed hardware resources by the programmable hardware element in performing the function. A deployment program deploys the hardware configuration program onto the programmable hardware element, where, after deployment, the device is operable to perform the function, where the programmable hardware element directly performs a first portion of the function, and the programmable hardware element invokes the fixed hardware resources to perform a second portion of the function. An optional measurement module couples to the device and performs signal conditioning and/or conversion logic on an acquired signal for the device.

French Abstract
L'invention concerne un systeme et un procede permettant de configurer un dispositif afin que celui-ci execute une fonction. Le dispositif comprend un element materiel programmable et une ou plusieurs ressources materielles fixes. Un programme est mis en memoire, celui-ci represente la fonction. Un programme de configuration materielle est genere en fonction du programme, il specifie une configuration de l'element materiel programmable executant la fonction, et l'utilisation desdites ressources materielles fixes par l'element materiel programmable lors de l'execution de la fonction. Un programme de deploiement deploie le programme de configuration materielle sur l'element materiel programmable; apres deploiement, le dispositif est operationnel pour executer la fonction. L'element materiel programmable execute directement une premiere partie de la fonction et l'element materiel programmable demande aux ressources materielles fixes d'executer une seconde partie de cette fonction. Un module de mesure eventuel est relie au dispositif et il execute une logique de pretraitement de signaux et/ou de conversion sur un signal acquis destine au dispositif.

Legal Status (Type, Date, Text)
Publication 20030227 A2 Without international search report and to be republished upon receipt of that report.

Main International Patent Class: **G06F**
Publication Language: English
Filing Language: English
Fulltext Availability:
  Detailed Description
  Claims
Fulltext Word Count: 18770

English Abstract
  In hardware, performing computations on a stream typically requires handshaking signals to provide flow control. Many different handshaking protocols are available, and they are typically implemented in an ad hoc manner suited to the current design. An approach according to the invention uses a subset of the possible flow-control protocols in an effort to achieve a maximum amount of flexibility and reusability, while requiring only a moderate level of overhead when compared to manually-designed systems.

French Abstract
  Dans le materiel informatique, la realisation de calculs sur un flux requiert generalement des signaux d'etablissement de liaison afin de reguler le debit. De nombreux protocoles de transfert sont disponibles, qui sont generalement mis en oeuvre ad hoc, adaptes a la finalite de circonstance. Une approche selon l'invention fait appel a un sous-ensemble des protocoles possibles de regulation de debit afin d'atteindre un taux maximum de flexibilite et de reutilisation, tout en n'utilisant qu'un faible taux de surdebit, compare aux systemes manuellement concus.

Legal Status (Type, Date, Text)
Publication 20021205 A2 Without international search report and to be republished upon receipt of that report.

11/5/9 (Item 9 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00948125 **Image available**
FPGA COPROCESSING SYSTEM
SYSTEME FPGA DE CO-TRAITEMENT
Patent Applicant/Assignee:
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  CELOXICA HOLDINGS PLC, 20 Park Gate, Milton Park, Abingdon, Oxon OX14 4SH , GB, GB (Residence), GB (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
  NOYES Gareth, Abingdon, GB, GB (Residence), GB (Nationality), (Designated only for: US)
  NEWTON Stuart, Oxford, GB, GB (Residence), GB (Nationality), (Designated only for: US)
  ALEXANDER John, Oxford, GB, GB (Residence), GB (Nationality), (Designated only for: US)
  HAMID Hammad, Berkshire, GB, GB (Residence), GB (Nationality), (Designated only for: US)
  NEWMAN Mat, Oxford, GB, GB (Residence), GB (Nationality), (Designated only for: US)
  SWEENEY Charles, Didcot, GB, GB (Residence), GB (Nationality), (Designated only for: US)
Legal Representative:
  DAVIDSON Clifford M (et al) (agent), Davidson, Davidson & Kappel, LLC, 14th floor, 485 Seventh Avenue, New York, NY 10018, US,
Patent and Priority Information (Country, Number, Date):
  Patent: WO 200282267 A1 20021017 (WO 0282267)
  Application: WO 2002US10611 20020404 (PCT/WO US0210611)
  Priority Application: US 2001281943 20010406
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU

CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS KE KG KP
KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD
SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-009/54**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 10292

English Abstract
A system is provided which includes a host computing environment (1) and a field programmable gate array ("FPGA") (2). The host computing environment (1) includes a compiled software application which, in turn, includes a first plurality of functions and a second plurality of function calls. The FPGA (2) is coupled to the host computing environment (1), and includes a compiled user function which is executed in response to one of the second plurality of function calls.

French Abstract
L'invention porte sur un systeme comprenant un environnement informatique central (1) et une matrice prediffusee programmable (<= FPGA >=) (2). Cet environnement (1) comporte une application logiciel compilee qui comporte elle-meme une premiere pluralite de fonctions et une seconde pluralite d'appels de fonction. La matrice FPGA (2) est couplee a l'environnement informatique central (1) et comporte une fonction utilisateur compilee qui est executee en reponse a la seconde pluralite d'un des appels de fonction.

Legal Status (Type, Date, Text)
Publication 20021017 A1 With international search report.

11/5/10 (Item 10 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00929467 **Image available**
SYSTEM AND METHOD FOR DESIGNING INTEGRATED CIRCUITS
SYSTEME ET PROCEDE POUR CONCEVOIR DES CIRCUITS INTEGRES
Patent Applicant/Assignee:
EXPERIENCE FIRST INC, 3275 Stevens Creek Boulevard, Suite 220, San Jose, CA 95117, US, US (Residence), US (Nationality)
Inventor(s):
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Legal Representative:
TEST Aldo J (et al) (agent), Flehr Hohbach Test Albritton & Herbert LLP, 4 Embarcadero Center, Suite 3400, San Francisco, CA 94111-4187, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200263509 A1 20020815 (WO 0263509)
Application: WO 2002US3937 20020206 (PCT/WO US0203937)
Priority Application: US 2001778182 20010206
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU
CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP
KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO
RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZM ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-017/50**
International Patent Class: **G06F-009/44** ; **G06F-013/10** ; **G06F-013/12** ; H03K-019/00

Publication Language: English
Filing Language: English
Fulltext Availability:
  Detailed Description
  Claims
Fulltext Word Count: 6175

English Abstract
  A system (100) and method are provided for developing customised integrated circuits (ICs) for use in an external system (105) while connected to the external system. In one embodiment, the system (100) includes a development board (115) for holding an IC core (120), the board having several ports (125) for transmitting signals to and from the IC core. A computer (130) with hardware descriptor language (HDL) software running thereon, coupled to the development board to configure the IC core to form the IC. Interface software (180), also running on the computer (130), translates Register Transfer Level (RTL) code entered by a designer to code used by the HDL software, (180) includes program code for enabling the designer to (i) assign predetermined signals in the RTL code to predetermined ports (125); (ii) assigns a clock speed for the IC core (120); determine if the IC core can operate at the assigned clock speed; (iii) designated the ports to be monitored; and (iv) designate an output to be recorded in a VCD file.

French Abstract
  L'invention concerne un systeme (100) et un procede pour developper des circuits integres personnalises (CI) destines a etre utilises dans un systeme exterieur (105) lorsqu'ils sont connectes a ce systeme exterieur. Dans un mode de realisation, le systeme (100) comprend une carte de developpement (115) pour contenir un coeur de circuits integres (120), cette carte possedant plusieurs ports (125) pour transmettre des signaux vers et a partir du coeur de circuits integres. Un ordinateur (130) avec un logiciel de langage de descripteur de materiel (HDL) est couple a la carte de developpement pour configurer le coeur de circuits integres afin de former les circuits integres. Un logiciel d'interface (180), fonctionnant egalement sur l'ordinateur (130), traduit un code de niveau de transfert de registre (RTL) introduit par un concepteur en un code utilise par le logiciel HDL (180) et comprend un code de programme pour permettre au concepteur (i) d'attribuer des signaux predetermines dans le code RTL a des ports predetermines (125), (ii) d'attribuer une vitesse d'horloge pour le coeur de circuits imprimes (120), de determiner si le coeur de circuits imprimes peut fonctionner a la vitesse d'horloge attribuee, (iii) de designer les ports a surveiller, et (iv) de designer une sortie a enregistrer dans un fichier VCD.

Legal Status (Type, Date, Text)
Publication 20020815 A1 With international search report.
Examination 20021114 Request for preliminary examination prior to end of 19th month from priority date

11/5/11 (Item 11 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00927555 **Image available**
SYSTEM, METHOD AND ARTICLE OF MANUFACTURE FOR SIMULTANEOUSLY GENERATING NETLISTS WITH MULTIPLE FORMATS
SYSTEME, PROCEDE ET ARTICLE MANUFACTURE PERMETTANT DE GENERER SIMULTANEMENT DES LISTES D'INTERCONNEXIONS DANS DE NOMBREUX FORMATS
Patent Applicant/Assignee:
  CELOXICA LIMITED, 7 Milton Park, Abingdon, Oxfordshire OX14 4RT, GB, GB (Residence), GB (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
  BOWEN Matt, 47 Surman House, Mandelbrote Drive, Littlemore, Oxford OX4 4XG, GB, GB (Residence), GB (Nationality), (Designated only for: US)
Legal Representative:
  NICHOLLS Michael John (et al) (agent), J.A. Kemp & Co., 14 South Square,

Gray's Inn, London WC1R [redacted], GB,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200261634 A2 20020808 (WO 0261634)
Application: WO 2002GB386 20020129 (PCT/WO GB0200386)
Priority Application: US 2001772551 20010129
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG US UZ VN YU ZA ZM ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-017/50**
Publication Language: English
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Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 4776

English Abstract
A system, method and article of manufacture are provided for compiling a computer program for programming a hardware device. In general, a first net list is created with a first format based on a computer program and a second net list is created with a second format based on the computer program. The first net list and the second net list are created utilizing a single compiler.

French Abstract
La presente invention concerne un systeme, un procede et un article manufacture qui permettent de compiler un programme d'ordinateur servant a programmer un dispositif materiel. En general, une premiere liste d'interconnexions est creee dans un premier format en fonction d'un programme d'ordinateur et une deuxieme liste d'interconnexions est creee dans un deuxieme format en fonction du programme d'ordinateur. Les premiere et deuxieme listes d'interconnexions sont creees a l'aide d'un seul et unique compilateur.

Legal Status (Type, Date, Text)
Publication 20020808 A2 Without international search report and to be republished upon receipt of that report.

11/5/12 (Item 12 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00927501 **Image available**
SYSTEM, METHOD AND ARTICLE OF MANUFACTURE FOR INTERFACE CONSTRUCTS IN A PROGRAMMING LANGUAGE CAPABLE OF PROGRAMMING HARDWARE ARCHITECTURES
SYSTEME, PROCEDE ET ARTICLE MANUFACTURE POUR DES CONSTRUCTIONS D'INTERFACE DANS UN LANGAGE DE PROGRAMMATION CAPABLE DE PROGRAMMER DES ARCHITECTURES DE MATERIEL
Patent Applicant/Assignee:
CELOXICA LIMITED, 7 Milton Park, Abingdon, Oxfordshire OX14 4RT, GB, GB (Residence), GB (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
BOWEN Matt, 47 Surman House, Mandelbrote Drive, Littlemore, Oxford OX4 4XG, GB, GB (Residence), GB (Nationality), (Designated only for: US)
Legal Representative:
NICHOLLS Michael John (et al) (agent), J.A. Kemp & Co., 14 South Square, Gray's Inn, London WC1R 5JJ, GB,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200261576 A2 20020808 (WO 0261576)
Application: WO 2002GB379 20020129 (PCT/WO GB0200379)
Priority Application: US 2001772555 20010129
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU

CZ DE DK DM DZ EC EE ES FI GD GE GH GM HR HU ID IL IN IS KE KG KP
KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO
RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG US UZ VN YU ZA ZM ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-009/44**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 9771

English Abstract
A system, method and article of manufacture are provided for using a versatile interface. First computer code is written in a first programming language. Included in the first computer code is reference to second computer code in a second programming language. The second computer code is simulated for use during the execution of the first computer code in the first programming language.
French Abstract
L'invention concerne un systeme, un procede et un article manufacture pour utiliser une interface polyvalente. Un premier code machine est ecrit dans un premier langage de programmation. Dans ce premier code machine est incluse une reference a un second code machine dans un second langage de programmation. Le second code machine est simule pour une utilisation durant l'execution du premier code machine dans le premier langage de programmation.

Legal Status (Type, Date, Text)
Publication 20020808 A2 Without international search report and to be republished upon receipt of that report.

11/5/13 (Item 13 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00878807 **Image available**
AN ARRAY OF PARALLEL PROGRAMMABLE PROCESSING ENGINES AND DETERMINISTIC METHOD OF OPERATING THE SAME
RESEAU DE MOTEURS DE TRAITEMENT PROGRAMMABLES PARALLELES ET PROCEDE DETERMINISTE DE MISE EN OEUVRE DE CE RESEAU
Patent Applicant/Assignee:
EASICS NV, Interleuvenlaan 86, B-3001 Leuven, BE, BE (Residence), BE (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
VANDEWEERD Ivo, Vuurkruisenlaan 1, B-3500 Hasselt, BE, BE (Residence), BE (Nationality), (Designated only for: US)
Legal Representative:
HERTOGHE Kris (et al) (agent), Bird Goen & Co., Vilvoordsebaan 92, B-3020 Winksele, BE,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200212999 A2-A3 20020214 (WO 0212999)
Application: WO 2001BE134 20010808 (PCT/WO BE0100134)
Priority Application: GB 200019341 20000808
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-017/50**
International Patent Class: **G06F-009/44**

Publication Language: English
Filing Language: English
Fulltext Availability:
  Detailed Description
  Claims
Fulltext Word Count: 26391

English Abstract
  The present invention provides an array of parallel programmable processing engines interconnected by a switching network. At least some of the processing engines execute a thread, and at least some threads communicate with each other through communication objects either internally within one processing engine or through the network. A scheduling step of the parallel programmable processing engines is initiated by one or more events, an event being defined by a change of a state variable of a communication object. The array comprises: means for scheduling a scheduling step of the processing engines, the scheduling means comprising means for executing at least a first set of threads in parallel, means for updating state values of communications objects in response to the parallel executing step, and means for repeatedly and sequentially scheduling the executing means and the updating means until no more events occur. The present invention also provides a deterministic method of operating such an array.

French Abstract
  La presente invention concerne un reseau de moteurs de traitement programmables paralleles interconnectes par un reseau de commutation. Au moins certains moteurs de traitement executent une unite d'execution, et au moins certaines unites d'execution communiquent entre elles au moyen d'elements de communication, lesdites communications etant soit realisees de maniere interne dans un moteur de traitement, soit par l'intermediaire du reseau. Une etape d'ordonnancement des moteurs de traitement programmables paralleles est mise en route par l'intermediaire d'un ou plusieurs evenements, un evenement etant defini par un changement d'une variable d'etat d'un element de communication. Ledit reseau est compose de moyens destines a ordonnancer une etape d'ordonnancement des moteurs de traitement, ces moyens d'ordonnancement comportant des moyens destines a executer au moins un premier ensemble d'unites d'execution en parallele ; de moyens destines a actualiser des valeurs d'etat d'elements de communication en reponse a l'etape d'execution en parallele ; et, de moyens destines a ordonnancer de maniere repetee et sequentielle les moyens d'execution et les moyens d'actualisation jusqu'a ce qu'aucun evenement ne se produise plus. La presente invention concerne egalement un procede deterministe de mise en oeuvre d'un tel reseau.

Legal Status (Type, Date, Text)
Publication 20020214 A2 Without international search report and to be republished upon receipt of that report.
Search Rpt 20020502 Late publication of international search report
Republication 20020502 A3 With international search report.
Republication 20020502 A3 Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.
Examination 20020510 Request for preliminary examination prior to end of 19th month from priority date

11/5/14 (Item 14 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00830054 **Image available**
DIGITAL CIRCUIT IMPLEMENTATION BY MEANS OF PARALLEL SEQUENCERS
MISE EN OEUVRE D'UN CIRCUIT NUMERIQUE AU MOYEN DE SEQUENCEURS PARALLELES
Patent Applicant/Inventor:
  HYDUKE Stanley M, 59 Gulf Stream Court, Las Vegas, NV 89113, US, US (Residence), US (Nationality)
Legal Representative:

domaine delta-sigma. Des operateurs lineaires sont configures pour fournir une fermeture en repondant a au moins deux criteres: (1) concernant les operateurs lineaires, au moins une (a) des entrees et (b) des sorties d'une partie de l'operateur utilise pour mettre en oeuvre une fonction mathematique est mise a l'echelle (c'est-a-dire normalisee) pour garantir des resultats valables, et (2) les valeurs de sortie de chaque fonction mathematique sont remodulees en un seul train de bits dans le domaine delta-sigma. En outre, des operateurs non lineaires tels que des operateurs mathematiques sont configures dans l'optique d'obtenir des resultats valables dans la region delta-sigma.

Legal Status (Type, Date, Text)
Publication 20000921 A1 With international search report.
Examination 20001123 Request for preliminary examination prior to end of 19th month from priority date

11/5/16 (Item 16 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00731108 **Image available**
FPGA INTEGRATED CIRCUIT HAVING EMBEDDED SRAM MEMORY BLOCKS AND INTERCONNECT CHANNEL FOR BROADCASTING ADDRESS AND CONTROL SIGNALS
CIRCUIT INTEGRE PREDIFFUSE PROGRAMMABLE COMPORTANT DES BLOCS MEMOIRE SRAM INCLUS ET UN CANAL D'INTERCONNEXION PERMETTANT DE DIFFUSER LES SIGNAUX D'ADRESSE ET DE COMMANDE
Patent Applicant/Assignee:
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Inventor(s):
AGRAWAL Om P, 891 Highlands Circle, Los Altos, CA 94024, US,
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SHARPE-GEISLER Bradley A, 1416 Dot Court, San Jose, CA 95120, US,
NGUYEN Bai, 2611 Kendrick Circle, San Jose, CA 95121, US,
Legal Representative:
FLIESLER Martin C (et al) (agent), Fliesler, Dubb, Meyer and Lovejoy LLP, Suite 400, Four Embarcadero Center, San Francisco, CA 94111-4156, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200044095 A2-A3 20000727 (WO 0044095)
Application: WO 2000US1482 20000120 (PCT/WO US0001482)
Priority Application: US 99235351 19990121
Designated States: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: H03K-019/177
International Patent Class: **G06F-017/50**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 32590

English Abstract
A field-programmable gate array device (FPGA) having plural rows and columns of logic function units (VGB's) further includes a plurality of embedded memory blocks, where each memory block is embedded in a corresponding row of logic function units. Each embedded memory block has an address port for capturing received address signals and a controls port for capturing supplied control signals. Interconnect resources are provided including a Memory Controls-conveying Interconnect Channel (MCIC) for conveying shared address and control signals to plural ones of

the memory blocks on a broadcast or narrowcast basis.

French Abstract
Dispositif circuit integre prediffuse programmable (FPGA), qui comprend plusieurs lignes et colonnes d'unites fonctionnelles logiques (VGB) et qui comporte une pluralite de blocs memoire inclus, chaque bloc memoire etant inclus dans la ligne correspondante des unites fonctionnelles logiques. Chaque bloc memoire inclus comporte un port d'adresses qui permet de recevoir les signaux d'adresse et un port de commandes qui permet d'emettre les signaux de commande. Le dispositif comporte egalement des ressources d'interconnexion, notamment un canal d'interconnexion de transport des commandes memoire (MCIC), qui amene les signaux d'adresse et de memoire partages a plusieurs blocs memoire sur la base d'une diffusion bande large ou d'une diffusion ciblee.

Legal Status (Type, Date, Text)

Publication	20000727	A2 Without international search report and to be republished upon receipt of that report.
Search Rpt	20001123	Late publication of international search report
Search Rpt	20001123	Late publication of international search report
Correction	20011018	Corrected version of Pamphlet: pages 1/25-25/25, drawings, replaced by new pages 1/27-27/27; due to late transmittal by the receiving Office
Republication	20011018	A3 With international search report.

11/5/17 (Item 17 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00579162 **Image available**
MULTITHREADED HDL LOGIC SIMULATOR
SIMULATEUR LOGIQUE MULTIFILIERE DU HDL
Patent Applicant/Assignee:
CHAN Terence,
Inventor(s):
CHAN Terence,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200042535 A1 20000720 (WO 0042535)
Application: WO 2000US853 20000112 (PCT/WO US0000853)
Priority Application: US 99229134 19990112
Designated States: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW GH GM KE LS MW SD SL SZ TZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
Main International Patent Class: **G06F-017/50**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 23800

English Abstract
A multi-threaded HDL logic simulator system (2) which executes an event driven logic simulation of circuit design. The hardware description language (HDL) is coded in VHDL or Verilog languages or a mixture of both languages. The simulation language can be run on a single-processor or multiprocessor platforms (25). The appropriate compiler (1) is selected based on the user specify HDL source file. The system (2) creates a master thread (40) and one or more slave treads (41) for executing the event driven logic simulation algorithm on the single or multiprocessor platform (25).

French Abstract
L'invention concerne un systeme de simulation logique (2) du langage HDL qui execute une simulation logique entrainee par les evenements d'une

conception de circuit. Le [redacted]gage de conception de circuits [redacted]DL) est code dans les langages VHDL ou Verilog ou dans un melange de ces langages. Le langage de simulation est concu pour tourner sur des plates-formes (25) multiprocesseur ou a processeur unique. On choisit un compilateur approprie (1) en se basant sur le fichier source de HDL indique par l'utilisateur. Le systeme (2) cree une filiere maitre (40) et une ou plusieurs filieres esclaves (41) pour executer l'algorithme de simulation logique entrainee par les evenements sur une plate-forme (25) multiprocesseur ou a processeur unique.

11/5/18 (Item 18 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT
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00574714 **Image available**

HARDWARE/SOFTWARE CODESIGN SYSTEM

SYSTEME A CONCEPTION MIXTE MATERIEL/LOGICIEL

Patent Applicant/Assignee:
DASH TECHNOLOGIES LIMITED,
SAUL Jonathan Martin,
AUBURY Matthew Philip,
Inventor(s):
SAUL Jonathan Martin,
AUBURY Matthew Philip,

Patent and Priority Information (Country, Number, Date):
Patent: WO 200038087 A1 20000629 (WO 0038087)
Application: WO 99GB4338 19991221 (PCT/WO GB9904338)
Priority Application: GB 9828381 19981222
Designated States: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW GH GM KE LS MW SD SL SZ TZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
Main International Patent Class: **G06F-017/50**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 13369

English Abstract
A hardware/software codesign system for making an electronic circuit which includes both dedicated hardware and software controlled resources. The codesign system receives a behavioural description of the target electronic system and automatically partitions the required functionality between hardware and software, while being able to vary the parameters (e.g. size or power) of the hardware and/or software. Thus, for instance, the hardware and the processor for the software can be formed on an FPGA, each being no bigger than is necessary to perform the desired functions. The codesign system outputs a description of the required processor (which can be in the form of a net list for placement on the FPGA), machine code to run on the processor, and a net list or register transfer level description of the necessary hardware. It is possible for the user to write some parts of the description of the target system at register transfer level to give closer control over the operation of the target system, and the user can specify theprocessor or processors to be used, and can change, for instance, the partitioner, compilers or speed estimators used in the codesign system. The automatic partitioning may be performed by using a genetic algorithm which estimates the performance of randomly generated different partitions and selects an optimal one of them.

French Abstract
L'invention concerne un systeme a conception mixte materiel/logiciel permettant de realiser un circuit electronique qui comprend a la fois des ressources specifiques commandees par materiel et des ressources

specifiques commandees par logiciel. Ce systeme a conception mixte recoit une description comportementale de la part du systeme electronique cible et repartit automatiquement les fonctions necessaires entre le materiel et le logiciel tout en etant capable de modifier les parametres (p. ex. dimension ou puissance) du materiel et/ou du logiciel. Ainsi le materiel et le processeur pour le logiciel peuvent par exemple etre formes sur un prediffuse programmable, chacun ne depassant pas la taille requise pour realiser les fonctions desirees. Le systeme a conception mixte sort une description du processeur requis (sous forme de liste d'interconnexions pour la disposition sur le prediffuse programmable), un code d'instructions fonctionnant sur le processeur, et une liste d'interconnexions ou une description a base d'instructions de transfert registre a registre du materiel necessaire. L'utilisateur peut ecrire certaines parties de la description du systeme cible de transfert registre a registre ce qui lui permet de mieux controler les operations du systeme cible et il peut indiquer le ou les processeur(s) devant etre utilise(s) et peut modifier par exemple le repartiteur, les compilateurs ou les estimateurs de vitesse utilises dans le systeme a conception mixte. La repartition automatique peut etre realisee au moyen d'un algorithme genetique qui estime la performance des differentes repartition generees de maniere aleatoire, et selectionne une repartition optimale parmi ces dernieres.

11/5/19 (Item 19 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00527711 **Image available**
FIELD PROGRAMMABLE GATE ARRAY (FPGA) EMULATOR FOR DEBUGGING SOFTWARE
EMULATEUR DE PREDIFFUSE PROGRAMMABLE (FPGA) POUR MISE AU POINT DE LOGICIEL
Patent Applicant/Assignee:
ADVANCED TECHNOLOGY MATERIALS INC,
Inventor(s):
BARNETT Philip C,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9959063 A1 19991118
Application: WO 99US10123 19990507 (PCT/WO US9910123)
Priority Application: US 9878872 19980514
Designated States: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Main International Patent Class: **G06F-011/00**
International Patent Class: **G06F-009/455**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 4983

English Abstract
An emulator is used to debug sofware operating on a target micro-controller in a target circuit environment. The emulator contains a field programmable gate array that is programmed to contain an emulated target micro-controller and an emulated monitoring circuit which monitors the operations of the micro-controller. The emulated target micro-controller receives signals from the target circuit environment. The signals from the target circuit environment are communicated to the emulated target micro-controller by one or more channels, such as a data channel and a timing channel. The number of channels is limited so that signals from the target environment do not degrade the performance of the emulator. A host computer contains a software debug program which works with the emulated monitoring circuit to monitor the emulated micro-controller. The FIELD PROGRAMMABLE GATE ARRAY is programmed to have the characteristics of one or more types of memory, for example ROM, PROM and EEPROM to emulate the different types of memory.

French Abstract
L'invention concerne l'utilisation d'un emulateur pour mettre au point un logiciel, qui agit sur un microregisseur cible dans un environnement

de circuit cible. L'emulateur contient un prediffuse programmable qui est programme de facon a contenir un microregisseur cible emule et un circuit de surveillance emule qui surveille les operations du microregisseur. Le microregisseur cible emule recoit des signaux provenant de l'environnement de circuit cible. Les signaux provenant de l'environnement de circuit cible sont communiques au microregisseur cible emule par un ou plusieurs canaux, tels qu'un canal de donnees et un canal de temporisation. Le nombre de canaux est limite de sorte que des signaux provenant de l'environnement cible ne degradent pas les performances de l'emulateur. Un ordinateur hote contient un programme de mise au point de logiciel qui coopere avec le circuit de surveillance emule pour surveiller le microregisseur emule. Le prediffuse programmable est programme de maniere a presenter les caracteristiques d'un ou de plusieurs types de memoire, par exemple ROM, PROM et EEPROM en vue d'emuler ces differents types de memoire.

11/5/20 (Item 20 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT
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00518041

A METHOD AND APPARATUS FOR EVALUATING SOFTWARE PROGRAMS FOR SEMICONDUCTOR CIRCUITS

PROCEDE ET APPAREIL D'EVALUATION DE PROGRAMMES LOGICIELS POUR DES CIRCUITS SEMICONDUCTEURS

Patent Applicant/Assignee:
ADVANCED TECHNOLOGY MATERIALS INC,
Inventor(s):
BARNETT Philip C,
GREEN Andrew,

Patent and Priority Information (Country, Number, Date):
Patent: WO 9949393 A1 19990930
Application: WO 99US6226 19990322 (PCT/WO US9906226)
Priority Application: US 9847809 19980324
Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH HU IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW GH GM KE LS MW SD SL SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
Main International Patent Class: **G06F-009/455**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 7242

English Abstract
A microcontroller software testing tool (100) for testing and debugging software for a target semiconductor circuit implemented as a dynamic link library (210). The microcontroller software testing tool (100) includes a simulator (300) for simulating the execution of the software program on the target semiconductor circuit and an emulator (400) to permit emulation before the actual silicon exists. The microcontroller software testing tool (100) includes a software development environment dynamic link library (220) monitors the estimated time to execute the software on the target semicondutor circuit and monitors the percentage of code that is executed during texting. In an emulation mode, the microcontroller software testing tool (100) utilizes a low-cost field programmable gate array programmed with a hardware description language description of the target semiconductor circuit. The features of the microcontroller software testing tool (100) are accessible by means of a data exchange protocol provided by the operating system.

French Abstract
L'invention concerne un outil (100) d'essai de logiciel de microprocesseur destine a l'essai et au deverminage d'un logiciel pour un

circuit semiconducteur cible configure comme une bibliotheque de liens dynamiques (210). L'outil (100) d'essai de logiciel de microprocesseur comprend un simulateur (300) destine a simuler l'execution du programme logiciel sur le circuit semiconducteur cible et un emulateur (400) permettant une emulation avant la fabrication du veritable silicium. L'outil (100) d'essai de logiciel de microprocesseur comprend une bibliotheque de liens dynamiques (220) d'environnement de developpement de logiciel, controle le temps estime d'execution du logiciel sur le circuit semiconducteur cible et controle le pourcentage de code execute pendant l'essai. Dans un mode d'emulation, l'outil (100) d'essai de logiciel de microprocesseur fait appel a un reseau prediffuse programmable de faible cout, programme avec un langage de description de materiel du circuit semiconducteur cible. Les caracteristiques de l'outil (100) d'essai de logiciel de microprocesseur sont accessibles au moyen d'un protocole d'echange de donnees fourni par le systeme d'exploitation.

11/5/21 (Item 21 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT
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00511778 **Image available**

A PACKET-SWITCHED MULTIPLE-ACCESS NETWORK SYSTEM WITH DISTRIBUTED FAIR PRIORITY QUEUING

SYSTEME POUR RESEAU A ACCES MULTIPLE ET A COMMUTATION PAR PAQUETS A FILE D'ATTENTE A PRIORITE EQUITABLEMENT REPARTIE

Patent Applicant/Assignee:
EPIGRAM INC,
Inventor(s):
HOLLOWAY John T,
TRACHEWSKY Jason,
PTASINSKI Henry,

Patent and Priority Information (Country, Number, Date):
Patent: WO 9943130 A1 19990826
Application: WO 99US3070 19990212 (PCT/WO US9903070)
Priority Application: US 9826884 19980219
Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW GH GM KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
Main International Patent Class: **H04L-012/407**
International Patent Class: **H04L-012/413 ; G06F-013/376**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 7462

English Abstract
A packet-switched multiple-access network system with a distributed fair priority queuing media access control protocol that provides multiple levels of priority of access and fair collision resolution with improved performance is disclosed. In one embodiment, the system provides high-speed transport of multimedia information on a shared channel. Further, in one embodiment, MAC level side-band signaling that is useful to other levels of the network protocol (e.g., the physical layer) is also provided.

French Abstract
L'invention porte sur un systeme ameliore pour reseau a acces multiple et a commutation par paquets utilisant un protocole de controle des acces aux supports a priorite d'attente equitablement repartie, presentant plusieurs niveaux d'acces et resolvant equitablement les collisions. Dans l'une de ses realisations, le systeme assure le transfert a haute vitesse des informations multisupports sur un canal partage. Dans une autre realisation, il recourt a une signalisation de controle des acces aux

supports a bande laterale [redacted] signalisation de niveaux, util[redacted] our d'autres niveaux du protocole (par exemple la couche physique) du reseau.

11/5/22 (Item 22 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT
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00478146 **Image available**

SYSTEM AND METHOD FOR CONVERTING GRAPHICAL PROGRAMS INTO HARDWARE IMPLEMENTATIONS

CONVERSION DE PROGRAMMES GRAPHIQUES EN REALISATIONS MATERIELLES ET SYSTEME CORRESPONDANT

Patent Applicant/Assignee:
NATIONAL INSTRUMENTS CORPORATION,
Inventor(s):
KODOSKY Jeffrey L,
ANDRADE Hugo,
ODOM Brian K,
BUTLER Cary P,

Patent and Priority Information (Country, Number, Date):
Patent: WO 9909498 A1 19990225
Application: WO 98US13040 19980622 (PCT/WO US9813040)
Priority Application: US 97912427 19970818
Designated States: CA JP AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Main International Patent Class: **G06F-017/50**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 21796

English Abstract
A computer-implemented system and method for generating a hardware implementation of graphical code. The method comprises first creating a graphical program. A first portion of the graphical program may optionally be compiled into machine code for execution by a CPU. A second portion of the graphical program is converted into a hardware implementation according to the present invention. The opertion of converting the graphical program into a hardware implementation comprises exporting the second portion of the graphical program into a hardware description, wherein the hardware description describes a hardware implementation of the second portion of the graphical program, and then configuring a programmable hardware element utilizing the hardware description to produce a configured hardware element. The configured hardware element thus implements a hardware implementation of the second portion of the graphical program.

French Abstract
La presente invention concerne un systeme et un procede informatique de generation de mise en oeuvre materielle de code graphique. Le procede consiste d'abord a creer un programme graphique. Une premiere partie du programme graphique peut eventuellement etre compilee en code machine pour execution par une UC. Une deuxieme partie du programme graphique est convertie en mise en oeuvre materielle conformement a la presente invention. L'operation de conversion du programme graphique en mise en oeuvre materielle consiste a exporter la deuxieme partie du programme graphique en une description materielle, laquelle description materielle decrit une mise en oeuvre materielle de la deuxieme partie du programme graphique. Le procede consiste ensuite a configurer un element materiel programmable en utilisant la description materielle afin de produire un element materiel configure. L'element materiel ainsi configure represente une mise en oeuvre materielle de la deuxieme partie du programme graphique.

11/5/23 (Item 23 from file: 349)

Publication Language: Englis
Fulltext Availability:
  Detailed Description
  Claims
Fulltext Word Count: 5054

English Abstract
Client-server software partitions Windows applications into multi-media and other less-observable instructions such that client may run audio/visual-related commands remotely, thereby appearing to client-user as when application where run solely by central server. Clients may access application through web-sites or remote access servers. Client requests may be atomized such that instruction set sub-sets are partitioned correspondingly. Operating system parameters on which application is run may be accessed selectably. Server may centralize client administration and provide metering of application usage.

French Abstract
On utilise un logiciel client-serveur qui segmente des applications sous Windows en instructions multimedias et en d'autres instructions moins visibles, de sorte que le client distant puisse executer localement des commandes relatives a la partie audio/visuelle, pour que l'application apparaisse au client-utilisateur comme si elle n'etait executee que par le serveur central. Les clients ont acces a l'application par l'intermediaire de sites sur le Web ou par l'intermediaire de serveurs d'acces a distance. Les requetes des clients peuvent etre "atomisees", pour que des sous-ensembles du jeu d'instructions soient segmentes de facon correspondante. Les parametres du systeme d'exploitation sous lesquels l'application est executee peuvent faire l'objet d'un acces selectif. Le serveur peut centraliser l'administration des clients et mesurer l'utilisation d'une application donnee.

11/5/25 (Item 25 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00406214 **Image available**
HARDWARE AND SOFTWARE DEVELOPMENT IN COMPUTER SYSTEMS HAVING MULTIPLE DISCRETE COMPONENTS
EXTENSION DE MATERIEL ET DE LOGICIEL DANS DES SYSTEMES INFORMATIQUES A PLUSIEURS COMPOSANTS SEPARES
Patent Applicant/Assignee:
  MICROSOFT CORPORATION,
Inventor(s):
  VOTH David W,
Patent and Priority Information (Country, Number, Date):
  Patent: WO 9746959 A1 19971211
  Application: WO 97US9290 19970528 (PCT/WO US9709290)
  Priority Application: US 96659084 19960603
Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE HU IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK TJ TM TR TT UA UG UZ VN GH KE LS MW SD SZ UG AM AZ BY KG KZ MD RU TJ TM AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG
Main International Patent Class: **G06F-017/50**
International Patent Class: **G06F-15:78 ; G06F-13:40**
Publication Language: English
Fulltext Availability:
  Detailed Description
  Claims
Fulltext Word Count: 10685

English Abstract
A computer system includes a plurality of discrete computer components and an integrated circuit that interfaces between the discrete computer components. The integrated circuit has internal hardware interfaces corresponding to respective discrete computer components. The internal

hardware interfaces are selected from a limited number of available pre-defined internal hardware interfaces for general kinds of computer components. The internal hardware interfaces are accessible only within the integrated circuit. The integrated circuit further includes component-specific hardware interfaces for connecting the individual discrete components to the selected pre-defined internal HDL interfaces. The component-specific hardware interfaces are designed individually for the different discrete computer components to interface the discrete components to the internal hardware interfaces. A development system is disclosed for use during development of such a computer system. The development system includes interconnections that allow functions to be easily moved from the integrated circuit to a system CPU.

French Abstract

L'invention concerne un systeme informatique comprenant une pluralite de composants informatiques separes et un circuit integre qui interface les composants informatiques separes. Le circuit integre comporte des interfaces materielles internes correspondant a des composants informatiques separes, respectifs. Les interfaces materielles internes sont selectionnees a partir d'un nombre limite d'interfaces materielles internes predefinies, disponibles, destinees a toutes sortes de composants informatiques. Les interfaces materielles internes sont accessibles uniquement dans le circuit integre. Ce circuit integre comprend egalement des interfaces materielles specifiques a des composants destinees a connecter les composants separes individuels aux interfaces HDL internes predefinies selectionnees. Les interfaces materielles specifiques a des composants sont concues individuellement pour differents composants informatiques separes afin d'interfacer les composants separes et les interfaces materielles internes. L'invention concerne egalement un systeme d'extension destine a etre utilise au cours de l'extension de ce type de systeme informatique. Ce systeme d'extension comporte des interconnexions qui facilitent le deplacement des fonctions du circuit integre a une unite centrale du systeme.

11/5/26 (Item 26 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT
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00387765 **Image available**

CONFIGURATION EMULATION OF A PROGRAMMABLE LOGIC DEVICE
EMULATION DE CONFIGURATION D'UNE UNITE LOGIQUE PROGRAMMABLE

Patent Applicant/Assignee:
XILINX INC,
Inventor(s):
BAXTER Glenn A,

Patent and Priority Information (Country, Number, Date):
Patent: WO 9728508 A1 19970807
Application: WO 97US1182 19970124 (PCT/WO US9701182)
Priority Application: US 96594933 19960131; US 96613785 19960229
Designated States: JP AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Main International Patent Class: **G06F-017/50**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 7586

English Abstract

A configuration emulation circuit generates configuration signals to emulate a Programmable Logic Device (PLD) in a configuration timing relationship and a configuration protocol relationship between a programming circuit and the PLD. The circuit includes a first circuit to emulate the PLD in the configuration timing relationship. The circuit also includes a second circuit to emulate the PLD in the configuration protocol relationship. The second circuit is coupled to receive a configuration mode signal and is responsive to the configuration mode signal.

French Abstract
La presente invention concerne un circuit d'emulation de configuration qui genere des signaux de configuration destines a emuler une Unite Logique Progammable (ULP) en conservant les relations de synchronisme de la configuration et les relations de protocole de la configuration entre un circuit de programmation et l'ULP. Le circuit est constitue d'un premier circuit destine a emuler l'ULP en conservant les relations de synchronisme de la configuration. Ce circuit est egalement constitue d'un second circuit destine a emuler l'ULP en conservant les relations de protocole de la configuration. Le second circuit, qui est couple pour recevoir un signal de mode de configuration, reagit a ce signal de mode de configuration.

11/5/27 (Item 27 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00281632
A METHOD FOR MODELING BIDIRECTIONAL OR MULTIPLICATIVELY DRIVEN SIGNAL PATHS IN A SYSTEM TO ACHIEVE A GENERAL PURPOSE STATICALLY SCHEDULED SIMULATOR
METHODE DE MODELISATION DE CHEMINS DE SIGNAUX BIDIRECTIONNELS OU A SOURCES MULTIPLES DANS UN SYSTEME, PERMETTANT DE REALISER UN SIMULATEUR A SEQUENCEMENT STATIQUE
Patent Applicant/Assignee:
COMDISCO SYSTEMS INC,
Inventor(s):
HERLITZ Lars G,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9429810 A1 19941222
Application: WO 94US6936 19940614 (PCT/WO US9406936)
Priority Application: US 9376015 19930614
Designated States: AT AU BB BG BR BY CA CH CN CZ DE DK ES FI GB HU JP KP KZ MG MN MW NL NO NZ PL PT RO RU SD SE SK UA UZ VN AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG
Main International Patent Class: **G06F-015/60**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 2253

English Abstract
A method is disclosed whereby systems having bidirectional and/or multiplicatively driven data paths are statically scheduled for simulation. The method flattens the netlist to convert bidirectional data flow paths into unidirectional, multiplicatively driven data paths. All drivers connected to multiplicatively driven data paths (or nets) are isolated from the net using a bus resolution block. The bus resolution block implements a resolution function which permits the system to be statically scheduled for simulation. Simulation speed is increased substantially thereby.

French Abstract
Cette methode prevoit le sequencement statique de systemes a chemins de donnees bidirectionnels et/ou a sources multiples et la reduction en elements simples de la liste des interconnexions pour convertir les chemins de flux de donnees bidirectionnels en chemins de donnees unidirectionnels a sources multiples. Tous les pilotes connectes aux chemins de donnees (ou aux reseaux) a sources multiples sont isoles du reseau au moyen d'un bloc de resolution de bus qui remplit une fonction de resolution permettant le sequencement statique du systeme aux fins de la simulation, ce qui accroit sensiblement la vitesse de cette derniere.

```
Set     Items   Description
S1       9339   ASIC OR FPGA OR PROGRAMMABLE()GATE()ARRAY OR PLC OR PLD OR
            PROGRAMMABLE()LOGIC()(DEVICE? OR CONTROL?)
S2        122   VHDL OR VERY()HIGH()SPEED()INTEGRATED()CIRCUIT()DESCRIPTION
S3    1278334   CONVERT? OR CONVERS? OR TRANSLAT? OR TRANSFORM? OR COMPIL?
S4          0   DC2NCF AND S2
S5          6   S1 AND S2 AND S3
S6         13   S1 AND S2
S7         13   IDPAT (sorted in duplicate/non-duplicate order)
S8         13   IDPAT (primary/non-duplicate records only)
File 344:Chinese Patents Abs Aug 1985-2003/Jan
         (c) 2003 European Patent Office
File 347:JAPIO Oct 1976-2002/Dec(Updated 030402)
         (c) 2003 JPO & JAPIO
File 350:Derwent WPIX 1963-2003/UD,UM &UP=200328
         (c) 2003  Thomson Derwent
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8/5/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2003 Thomson Derwent. All rts. reserv.

014834367 **Image available**
WPI Acc No: 2002-655073/200270
Related WPI Acc No: 2001-396653; 2002-581981
XRPX Acc No: N02-517605
Process structured layout of design objects in a hardware description language involves providing first design objects in VHDL in which first design objects have no input ports and no output ports
Patent Assignee: XILINX INC (XILI-N)
Inventor: HWANG L J; MITRA S; PATTERSON C D
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6430732	B1	20020806	US 9849598	A	19980327	200270	B
			US 99246253	A	19990208		

Priority Applications (No Type Date): US 99246253 A 19990208; US 9849598 A 19980327
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6430732	B1		13	G06F-017/50	CIP of application US 9849598 CIP of patent US 6237129

Abstract (Basic): US 6430732 B1
NOVELTY - The method involves providing first design objects in a very high-speed integrate circuit hardware description language (**VHDL**). The first design objects are compiled with a set of design objects, in which the first design objects have no input ports and no output ports.
DETAILED DESCRIPTION - The set of design objects are declared as elements within the first design objects, in which one or more of the set of design objects have input ports and output ports. Values to attributes of the first design objects are assigned, in which the values of attributes indicate the placement for the set of design objects within the first design objects.
USE - Process structured layout of design objects in a hardware description language (HDL). Applicable to a variety of systems for laying out designs for **programmable logic devices** .
ADVANTAGE - Provides placement directives that do not require coordinate-based specification of design objects, thereby alleviating the involved and error-prone specification and maintenance of coordinates for a complex hierarchical design.
DESCRIPTION OF DRAWING(S) - The figure is a block diagram that illustrates how the placement directives can be used in an example system.
pp; 13 DwgNo 1/5
Title Terms: PROCESS; STRUCTURE; LAYOUT; DESIGN; OBJECT; HARDWARE; DESCRIBE ; LANGUAGE; FIRST; DESIGN; OBJECT; FIRST; DESIGN; OBJECT; NO; INPUT; PORT ; NO; OUTPUT; PORT
Derwent Class: T01
International Patent Class (Main): G06F-017/50
International Patent Class (Additional): G06F-009/455
File Segment: EPI

8/5/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2003 Thomson Derwent. All rts. reserv.

014669924 **Image available**
WPI Acc No: 2002-490628/200252
XRPX Acc No: N02-387841
Relational content addressable memory e.g. for ASICs uses XOR logic circuits to compare equality of stored bits with respective bit of multibit input data word for routing to output

Patent Assignee: GRAY K S (GR[redacted]I); KONINK PHILIPS ELECTRONICS [redacted] (PHIG)
Inventor: GRAY K S; GRAY K
Number of Countries: 022 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200249038	A1	20020620	WO 2001IB2303	A	20011205	200252	B
US 20020105821	A1	20020808	US 2000736498	A	20001213	200254	
US 6483732	B2	20021119	US 2000736498	A	20001213	200280	

Priority Applications (No Type Date): US 2000736498 A 20001213
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200249038	A1	E	17	G11C-015/04	
Designated States (National): JP KR					
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR					
US 20020105821	A1			G11C-015/00	
US 6483732	B2			G11C-015/00	

Abstract (Basic): WO 200249038 A1

NOVELTY - The content addressable memory (CAMs) cells (40) have a data bus (DI) providing a multibit input data word, and generate a relational state bit output (T0, T0') dependent on a stored memory location (30) and the equality of the successive bits and most significant bits (DN). The input bits (D0, D0') are routed to the output if they are unequal with corresponding significant bits, using inverters (32), relational logic circuits (52) and selection logic including an XOR operator with four active-high/low gates using e.g. PMOS/NMOS IGFETs respectively.

DETAILED DESCRIPTION - The e.g. **ASIC** can be defined using macros through a Hardware Development Language (HDL) e.g. Verilog or **VHDL** , and the CAM cells can have true and complement bit storage nodes e.g. six transistor SRAM or four transistor/twin-cell DRAM, or be two or more separate ICs. A pass-transistor can be utilized in an IGFET gate implementation to buffer or re-drive the relational line (RL) at periodic logic pathway intervals e.g. every 3-5 logic circuits depending on desired performance. The data bus can be internal or external, serial or parallel, or a combination of both, and the relational operation is parallel, bit-by-bit.

An INDEPENDENT CLAIM is also included for a method of operating a CAM.

USE - For e.g. redundant back-up memory systems for Application Specific Integrated Circuits (ASICs), associative caches and databases.

ADVANTAGE - Permits full rail-to-rail operation of XOR logic for each logic circuit, allowing use with low-voltage memory cells. The CAM cell logic can be provided from existing HDL macros, and the repetitive inequality logic can be a separate macro, minimizing the need for existing CAM cell macro redesign.

DESCRIPTION OF DRAWING(S) - The drawing shows a schematic view of the CAM.

Memory location (30)
Inverters (32)
CAMs (40)
Relational logic circuits (52)
Data bus (DI)
Most significant bit (DN)
Input pairs (D0, D0'))
Relational line (RL)
True and complement output bits (T0, T0'))
pp; 17 DwgNo 1/2

Title Terms: RELATED; CONTENT; ADDRESS; MEMORY; EXCLUSIVE-OR; LOGIC; CIRCUIT; COMPARE; EQUAL; STORAGE; BIT; RESPECTIVE; BIT; MULTIBIT; INPUT; DATA; WORD; ROUTE; OUTPUT
Derwent Class: U13; U14
International Patent Class (Main): G11C-015/00; G11C-015/04
File Segment: EPI

8/5/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014309393 **Image available**
WPI Acc No: 2002-130096/200217
XRPX Acc No: N02-098141
Design tool for printed circuit board, generates hardware description language model which is identical in connectivity to PCB, based on netlist generated from components of PCB
Patent Assignee: STRALEN N A V (STRA-I)
Inventor: STRALEN N A V
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020004931	A1	20020110	US 2000188512	P	20000310	200217 B
			US 2001803431	A	20010309	

Priority Applications (No Type Date): US 2000188512 P 20000310; US 2001803431 A 20010309
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020004931	A1		13	G06F-017/50	Provisional application US 2000188512

Abstract (Basic): US 20020004931 A1
NOVELTY - A processor processes the entered descriptions, instances and interconnections of the components of the PCB to generate an internal netlist. A compiler processes description, instances, interconnections and the generated internal netlist to generate a very high speed integrated circuit hardware description language (**VHDL**) model which is identical in connectivity to the PCB.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for printed circuit board hardware description language model creation method.
USE - For designing printed circuit board (PCB) including application specific integrated circuit (**ASIC**), field **programmable gate array** (**FPGA**).
ADVANTAGE - Since the **VHDL** board model is identical with the actual PCB, and cross-checked against the netlist from board layout, the risk of board re-design is reduced, hence board design quality is improved, reducing the time of integration and design of the PCB.
DESCRIPTION OF DRAWING(S) - The figure explains the process of designing PCB using design tool.
pp; 13 DwgNo 2/5
Title Terms: DESIGN; TOOL; PRINT; CIRCUIT; BOARD; GENERATE; HARDWARE; DESCRIBE; LANGUAGE; MODEL; IDENTICAL; CONNECT; PCB; BASED; GENERATE; COMPONENT; PCB
Derwent Class: T01
International Patent Class (Main): G06F-017/50
File Segment: EPI

8/5/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014245045 **Image available**
WPI Acc No: 2002-065745/200209
Related WPI Acc No: 2001-145965
XRPX Acc No: N02-048828
Integrated circuit design method e.g. for application specific integrated circuit, involves dividing circuit into multiple modules to which buffer modules are defined
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: BROWN J R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week

US 6327692 B1 20011204 US 97971974 A 19971117 200205 B
US 2000663322 A 20000915

Priority Applications (No Type Date): US 97971974 A 19971117; US 2000663322 A 20000915
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 6327692 B1 14 G06F-017/50 Cont of application US 97971974
Cont of patent US 6148432

Abstract (Basic): US 6327692 B1
NOVELTY - A circuit is divided into multiple modules (516,518) including inputs and outputs. A buffer module (514) is defined as ring surrounding a circuit module, so that a set of output signals from the circuit module passes through drivers in buffer module without any variation. Several designs are created for the circuit and buffer modules in high level design language, based on which a circuit is synthesized.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(a) Medium storing computer readable circuit design program;
(b) Circuit designing apparatus
USE - For designing application specific integrated circuits (**ASIC**), very high speed integrated circuit (VHIC) hardware description language (**VHDL**), using computer aided design (CAD) tools in workstation, personal computer, mainframe computer, super computer and drive controllers connected to server through networks such as local area network, ethernet or Token ring networks, wide area networks.
ADVANTAGE - Since the circuit is divided into several modules, the number of critical signals flowing between modules are minimized, and the characteristics of output critical signals are not changes, by changing the constraints on input and output signals, and by changing the circuitry within the modules and hence design time of circuit is reduced efficiently and signals are routed optimally between the modules.
DESCRIPTION OF DRAWING(S) - The figures show the flowchart explaining the circuit design method and the block diagram of a circuit.
Buffer module (514)
Modules (516,518)
pp; 14 DwgNo 3, 5/6
Title Terms: INTEGRATE; CIRCUIT; DESIGN; METHOD; APPLY; SPECIFIC; INTEGRATE ; CIRCUIT; DIVIDE; CIRCUIT; MULTIPLE; MODULE; BUFFER; MODULE; DEFINE
Derwent Class: T01
International Patent Class (Main): G06F-017/50
File Segment: EPI

8/5/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014219997 **Image available**
WPI Acc No: 2002-040695/200205
XRPX Acc No: N02-030171
C-type programming converting method for hardware design implementation, involves creating algorithmic expression in C-type programming language corresponding to preliminary hardware design
Patent Assignee: SYNETRY CORP (SYNE-N)
Inventor: COLEMAN D R; PANCHUL Y V; SODERMAN D A
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
US 20010034876 A1 20011025 US 97931148 A 19970916 200205 B
US 2001846092 A 20010430

Priority Applications (No Type Date): US 97931148 A 19970916; US 2001846092 A 20010430

Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 20010034876 A1 109 G06F-017/50 Cont of application US 97931148
Cont of patent US 6226776

Abstract (Basic): US 20010034876 A1

NOVELTY - Algorithmic representation is created in C-type programming language corresponding to a preliminary hardware design. The C-type programming language preliminary hardware design is complied into hardware description language (HQL) synthesizable design.

USE - For converting a C-type programming languages including APL, Ada, Algol, B, Basic, Kernighan and Ritchie C, ANSI C, C++, CLOS, COBOL, Clu, Common Lisp, Coral, Dylan, Eiffel, Emacs Lisp, Forth, FORTRAN, IDL, Icon, Java, Jovial, Lisp, LOGO, ML, Modula, Oberon, Objective C, PL/I, PL/M, Pascal, Postscript, Prolog, Python, RTL, Rexx, SETL, Simula, Sather, Scheme, Small-talk, Standard ML, TCL, TRAC into a hardware design language including verilog, **VHDL** , ABEL, CUPL, AHDL, MACHYX and PALASM for hardware design implementation of digital circuits such as **FPGA** , **ASIC** or other programmable logic.

ADVANTAGE - Enables compilation any high level language that is translate to a C-type programming language, thereby obviating the need for the user to read manuals for creating work around for portions of high level programming language.

DESCRIPTION OF DRAWING(S) - The figure shows a flowchart of high level programming language compiling method.

pp; 109 DwgNo 2/27

Title Terms: TYPE; PROGRAM; CONVERT; METHOD; HARDWARE; DESIGN; IMPLEMENT; ALGORITHM; EXPRESS; TYPE; PROGRAM; LANGUAGE; CORRESPOND; PRELIMINARY; HARDWARE; DESIGN
Derwent Class: T01
International Patent Class (Main): G06F-017/50
File Segment: EPI

8/5/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014028287 **Image available**
WPI Acc No: 2001-512501/200156
Circuit of correcting waveform shaping and chattering
Patent Assignee: LG INFORMATION & COMMUNICATIONS LTD (GLDS)
Inventor: CHOI P H
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
KR 2001020017 A 20010315 KR 9936701 A 19990831 200156 B

Priority Applications (No Type Date): KR 9936701 A 19990831
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
KR 2001020017 A 1 H03K-005/01

Abstract (Basic): KR 2001020017 A

NOVELTY - A circuit of correcting waveform shaping and chattering is provided to eliminate waveform shaping and chattering or noises in the circuit triggered by a power-on or a switch using a simple **VHDL** (Hardware Description Language) clause without additional circuit extension.

DETAILED DESCRIPTION - The circuit includes a charger/discharger(20) and a **PLD** (**Programmable Logic Device**) device or PGA(**Programmable Gate Array** Device) device(30). Here, The charger/discharger(20) includes a resistance(R), capacitor(C), diode(D) and switch(SW) and charges or discharges current triggered by a power-on or the switch(SW). The **PLD** or PLA device(30) includes three D-FlipFlops(31-33) and a comparator(34). The **PLD** or PLA(30) compares an input signal from the charger/discharger(30) with the signal's three consecutive latched values responding to a clock. And if the latched values are all the same as HIGH, the **PLD** or PLA

device(30) produces a HIGH signal. And if the latched values are all the same as LOW, the device(30) produces a LOW signal.
pp; 1 DwgNo 1/10
Title Terms: CIRCUIT; CORRECT; WAVEFORM; SHAPE; CHATTER
Derwent Class: U22
International Patent Class (Main): H03K-005/01
File Segment: EPI

8/5/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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013978516 **Image available**
WPI Acc No: 2001-462730/200150
Apparatus for transceiving data
Patent Assignee: MERCURY CORP (MERC-N)
Inventor: KIM H G
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 2001004869	A	20010115	KR 9925627	A	19990630	200150	B

Priority Applications (No Type Date): KR 9925627 A 19990630
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2001004869	A		1	H04L-012/28	

Abstract (Basic): KR 2001004869 A
NOVELTY - An apparatus for transceiving data is provided to transmit data stored in dual port memories to an external system by using a very high speed integrated circuit hardware description language(**VHDL**) program for an embedded **programmable logic device** (EPLD), or to receive data transmitted from the external system to store the received data in the dual port memories, so as to perform data transceiving processes at a high speed.
DETAILED DESCRIPTION - An input/output(I/O) controller(10) controls an internal and an external system, to make the internal/the external system access each of data. Dual port memories(12,16) access data in the internal system through one port, and access the data in the external system through the other port, under control of the I/O controller(10). I/O units(14,18) control data streams between the dual port memories(12,16) and the external system, under control of the I/O controller(10). A data I/O control function is set up in the I/O controller(10), by a very high speed integrated circuit hardware description language(**VHDL**) program for an embedded **programmable logic device** (EPLD).
pp; 1 DwgNo 1/10
Title Terms: APPARATUS; TRANSCEIVER; DATA
Derwent Class: W01
International Patent Class (Main): H04L-012/28
File Segment: EPI

8/5/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012881300 **Image available**
WPI Acc No: 2000-053134/200004
XRPX Acc No: N00-041393
Field programmable gate array **emulator for software debugging**
Patent Assignee: ADVANCED TECHNOLOGY MATERIALS (ADTE-N)
Inventor: BARNETT P C
Number of Countries: 020 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9959063	A1	19991118	WO 99US10123	A	19990507	200004	B

EP 1029275 A1 20000823 [redacted] 99920408 A 19990507 200041
WO 99US10123 A 19990507
US 6173419 B1 20010109 US 9878872 A 19980514 200104

Priority Applications (No Type Date): US 9878872 A 19980514
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
WO 9959063 A1 E 29 G06F-011/00
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
EP 1029275 A1 E G06F-011/00 Based on patent WO 9959063
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
US 6173419 B1 G06F-011/00

Abstract (Basic): WO 9959063 A1
NOVELTY - The emulator consists of a field **programmable gate array** (**FPGA**) that is programmed to contain an emulated target micro controller (92), and an emulated monitoring circuit (94) to regulate the operations of the micro controller. An emulator receives signals from a target circuit (96) through a predetermined number of channels so that deterioration in the performance of the emulator is prevented.
DETAILED DESCRIPTION - A logic description provided in a silicon design software language such as **VHDL** to program the micro controller and the emulator. The programs are stored in a host computer (98).
USE - For software debugging.
ADVANTAGE - Eliminates need for hardware modification by using existing hardware and hence reduces cost of device. Enhances software debugging process by using additional logic for monitoring circuit.
DESCRIPTION OF DRAWING(S) - The figure shows block diagram of an **FPGA** emulator.
Microcontroller (92)
Monitoring circuit (94)
Target circuit (96)
Host computer (98)
pp; 29 DwgNo 5/8
Title Terms: FIELD; PROGRAM; GATE; ARRAY; EMULATION; SOFTWARE; DEBUG
Derwent Class: T01
International Patent Class (Main): G06F-011/00
International Patent Class (Additional): G06F-009/455
File Segment: EPI

8/5/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012827619 **Image available**
WPI Acc No: 1999-633851/199954
XRPX Acc No: N99-468040
Evaluating genetic programming parse-trees using field programmable gate array **chip**
Patent Assignee: GTE INTERNETWORKING INC (SYLV)
Inventor: IYER S; MONTANA D J; MOORE S S B; POPP R L; VIDAVER G
Number of Countries: 019 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
WO 9953530 A2 19991021 WO 99US8048 A 19990413 199954 B

Priority Applications (No Type Date): US 9858786 A 19980413
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
WO 9953530 A2 E 16 H01L-000/00
Designated States (National): JP
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE

Abstract (Basic): WO 9953530 A2

NOVELTY - A very high speed integrated circuit hardware description language (**VHDL**) toolset (114) transforms a **VHDL** program specific into a gate-level net-list, which is then transformed into a technology-specific field **programmable gate array** (**FPGA**) description using a place and route tool. The primitive is transformed from a parse-tree and loaded onto the **FPGA** chip (122) from the computer (110) also including a genetic programming (GP) processing engine (112) and an evaluation and scoring unit (118). A database (116) stores program files for all GP primitives and the engine computes a score for that parse-tree after evaluating all nodes. The chip is remodeled by primitives to model different types of hardware configurations executing logic of the primitives.

DETAILED DESCRIPTION - AN INDEPENDENT CLAIM is included for a system for evaluating a parse-tree using **FPGA** chip.

USE - Evaluating parse-tree using **FPGA** chip.

ADVANTAGE - Automatically determines hardware designs at high speed without intervention.

DESCRIPTION OF DRAWING(S) - The drawing is a block diagram of a GP parse-tree evaluating system according to the present invention

VHDL toolset (114)

FPGA chip (122)

Evaluation and scoring unit (118)

Parse-tree database (116)

GP processing engine (112)

Computer (110)

pp; 16 DwgNo 1/3

Title Terms: EVALUATE; GENETIC; PROGRAM; PARSE; TREE; FIELD; PROGRAM; GATE; ARRAY; CHIP

Derwent Class: T01; U11; U21

International Patent Class (Main): H01L-000/00

File Segment: EPI

8/5/10 (Item 10 from file: 350)

DIALOG(R)File 350:Derwent WPIX
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012597948 **Image available**

WPI Acc No: 1999-404054/199934

XRPX Acc No: N99-301092

Test vector generating method for ASIC **design validation**

Patent Assignee: GENERAL ELECTRIC CO (GENE)

Inventor: HATFIELD W T; ITANI A M; LEUE W M

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5920830	A	19990706	US 97890273	A	19970709	199934	B

Priority Applications (No Type Date): US 97890273 A 19970709

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5920830	A		32	G01R-031/28	

Abstract (Basic): US 5920830 A

NOVELTY - Source code defining application specific integrated circuit to be tested, is written using very high speed integrated circuit hardware description language (**VHDL**). The code is preprocessed by scanning and extracting information to form a skeleton program, based on which data is compiled to generate at least one test vector to verify functionality of the **ASIC** circuit.

DETAILED DESCRIPTION - The **ASIC** circuit is simulated at a functional level to obtain functional level test data using the generated test vector. The circuit is simulated at a circuit level to obtain a circuit level test data output using the test vector. The functional level test data output is compared with circuit level test data output to generate a report which indicates timing and value errors. INDEPENDENT CLAIMS are also included for the following:

(a) test vector generating apparatus;

(b) method of translating **VHDL** code to executable code

USE - For **ASIC** design validation.

ADVANTAGE - The compiler eliminates tedious and time consuming process to generate different sets of test vectors for different levels of testing such as functional level and circuit level.

DESCRIPTION OF DRAWING(S) - The figure shows a data flow diagram illustrating operation of present tool sets for confirming **ASIC** designs.

pp; 32 DwgNo 1/3

Title Terms: TEST; VECTOR; GENERATE; METHOD; **ASIC** ; DESIGN; VALID
Derwent Class: S01; T01; U11; U13
International Patent Class (Main): G01R-031/28
International Patent Class (Additional): G06F-009/45; G06F-009/455
File Segment: EPI

8/5/11 (Item 11 from file: 350)

DIALOG(R)File 350:Derwent WPIX
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012374098 **Image available**
WPI Acc No: 1999-180205/199915
XRPX Acc No: N99-132361

Pullup or pulldown device modeling method in simulation modeling applications

Patent Assignee: XILINX INC (XILI-N)
Inventor: PATEL D
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5875111	A	19990223	US 97832318	A	19970325	199915	B

Priority Applications (No Type Date): US 97832318 A 19970325
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5875111	A		15	G06F-017/50	

Abstract (Basic): US 5875111 A

NOVELTY - The primitive procedure preserve the identity of selected states of input signal. The delayed and pre-mapped signal forms the input to a VITAL state table which is used to model the behavior of a pullup or pulldown device. The identity primitive procedure is then used to post-map the resulting signal in order to recover the selected states of the input signal.

DETAILED DESCRIPTION - An entity is modeled and identity primitive procedure which delays an input signal by a value specified in a timing generic and preserves the signal shape, is created. The created identity primitive procedure is used for premapping of input signal.

USE - For simulation modeling application.

ADVANTAGE - Selected states of input signal are preservable by performing pre-mapping and post-mapping of input signal.

DESCRIPTION OF DRAWING(S) - The figure shows the flow diagram of a VITAL pullup models with delay back annotation.

pp; 15 DwgNo 11/17

Title Terms: DEVICE; METHOD; SIMULATE; APPLY
Derwent Class: T01
International Patent Class (Main): G06F-017/50
File Segment: EPI

8/5/12 (Item 12 from file: 350)

DIALOG(R)File 350:Derwent WPIX
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010844916 **Image available**
WPI Acc No: 1996-341869/199634
XRPX Acc No: N96-287794

Integrated circuit mfr esp. for ASIC - using state machine extraction

of synchronous state machines from register-transfer level representation taken from scheduled behavioural hardware description language e.g. VERILOG (RTM) or VHDL

Patent Assignee: VLSI TECHNOLOGY INC (VLSI-N)
Inventor: GIOMI J; TARROUX G
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5537580	A	19960716	US 94362028	A	19941221	199634	B

Priority Applications (No Type Date): US 94362028 A 19941221
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5537580	A		20	G06F-017/00	

Abstract (Basic): US 5537580 A

The method includes the steps of describing the functionality of an integrated circuit in terms of a behavioral hardware description language, where the hardware description language describes behaviour which can be extracted as a state machine. A register level state machine transition table of the state machine is extracted from the hardware description language. A logic level state transition table representing the state machine is generated from the register level state machine description.

A state machine structural netlist representing the state machine is created from the logic level state transition table. The state machine structural netlist is combined with an independently synthesized structural netlist to create an integrated circuit structural netlist including the state machine to provide a basis for chip compilation, mask layout and integrated circuit fabrication.

USE/ADVANTAGE - VLSI and ULSI circuits. Improves efficiency of extraction of state machines from functional description of IC. More computationally efficient thus suitable for design of complex integrated circuits.

Dwg.1b/7

Title Terms: INTEGRATE; CIRCUIT; MANUFACTURE; **ASIC** ; STATE; MACHINE; EXTRACT; SYNCHRONOUS; STATE; MACHINE; REGISTER; TRANSFER; LEVEL; REPRESENT; SCHEDULE; BEHAVE; HARDWARE; DESCRIBE; LANGUAGE; RTM
Index Terms/Additional Words: APPLICATION; SPECIFIC; IC; CAD
Derwent Class: T01; U11
International Patent Class (Main): G06F-017/00
File Segment: EPI

8/5/13 (Item 13 from file: 347)

DIALOG(R)File 347:JAPIO
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07022194 **Image available**

SYSTEM LSI DEVELOPMENT SUPPORT SYSTEM AND RECORDING MEDIUM IN WHICH ITS PROGRAM FOR DEVELOPMENT SUPPORT IS RECORDED

PUB. NO.: 2001-249826 [JP 2001249826 A]
PUBLISHED: September 14, 2001 (20010914)
INVENTOR(s): MOGI KENJI
TANAKA RYOHEI
NAKAO TOSHIMITSU
APPLICANT(s): ROORAN KK
DAIHEN CORP
APPL. NO.: 2000-063308 [JP 200063308]
FILED: March 03, 2000 (20000303)
INTL CLASS: G06F-011/22; G06F-017/50

ABSTRACT

PROBLEM TO BE SOLVED: To make a test of a system LSI efficient and to shorten development period of the system LSI by enabling a production test of the entire system LSI constituted on a logical integrated circuit such as an **FPGA** as for a development support system of the system LSI.

SOLUTION: This system is constituted so as to generate a logic of a scan path at a **VHDL** level based on definition information on the scan path (#8). Thus, a scan path for operation verification of the entire system LSI is constructed by inputting the definition information on the scan path to a register and a memory to be required for the operation verification of the system LSI, and the production test of the entire system LSI is performed via the scan paths (#13).

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```
Set     Items   Description
S1     137837   ASIC OR FPGA OR PROGRAMMABLE()GATE()ARRAY OR PLC OR PLD OR
             PROGRAMMABLE()LOGIC()(DEVICE? OR CONTROL?)
S2       8633   VHDL OR VERY()HIGH()SPEED()INTEGRATED()CIRCUIT()DESCRIPTION
S3    3161816   CONVERT? OR CONVERS? OR TRANSLAT? OR TRANSFORM? OR COMPIL?
S4          0   DC2NCF AND S2
S5        403   S1 AND S2 AND S3
S6       1669   S1 AND S2
S7        102   S2(5N)S3 AND S1
S8         74   RD (unique items)
S9         50   S1(5N)S2(5N)S3
S10        25   S8 AND S9
File   8:Ei Compendex(R) 1970-2003/Apr W3
         (c) 2003 Elsevier Eng.  Info. Inc.
File  35:Dissertation Abs Online 1861-2003/Apr
         (c) 2003 ProQuest Info&Learning
File  65:Inside Conferences 1993-2003/Apr W4
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File   2:INSPEC 1969-2003/Apr W4
         (c) 2003 Institution of Electrical Engineers
File  94:JICST-EPlus 1985-2003/Apr W4
         (c)2003 Japan Science and Tech Corp(JST)
File 111:TGG Natl.Newspaper Index(SM) 1979-2003/May 02
         (c) 2003 The Gale Group
File 233:Internet & Personal Comp. Abs. 1981-2003/Apr
         (c) 2003 Info. Today Inc.
File   6:NTIS 1964-2003/May W1
         (c) 2003 NTIS, Intl Cpyrght All Rights Res
File 144:Pascal 1973-2003/Apr W4
         (c) 2003 INIST/CNRS
File  34:SciSearch(R) Cited Ref Sci 1990-2003/Apr W4
         (c) 2003 Inst for Sci Info
File  99:Wilson Appl. Sci & Tech Abs 1983-2003/Mar
         (c) 2003 The HW Wilson Co
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10/5/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
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05120390 E.I. No: EIP98094382105
Title: Rapid prototype of a fast data encryption standard with integrity processing for cryptographic applications
Author: Guendouz, Hassina; Bouaziz, Samir
Conference Title: Proceedings of the 1998 IEEE International Symposium on Circuits and Systems, ISCAS. Part 6 (of 6)
Conference Location: Monterey, CA, USA Conference Date: 19980531-19980603
Sponsor: IEEE
E.I. Conference No.: 48950
Source: Proceedings - IEEE International Symposium on Circuits and Systems v 6 1998. IEEE, Piscataway, NJ, USA,98CH36187. p 434-437
Publication Year: 1998
CODEN: PICSDI ISSN: 0271-4310
Language: English
Document Type: CA; (Conference Article) Treatment: A; (Applications); T ; (Theoretical)
Journal Announcement: 9811W2
Abstract: In this paper we present the design of a chip for real-time cryptographic processing in industrial applications. The chip acts as a co-processor of a system for the automatic ciphering and data integrity processing: it implements the DES/MAC algorithm (Data Encryption Standard/Message Authentication Code) in the same silicon area with high speed performance. These research come within a process aiming at reaching an implementation onto specialized pipeline and parallel architecture from algorithm specification. The design has been performed in rapid prototype ACTEL **Programmable Gate Array** Device using an approach based on high level **transformations** on the **VHDL** specifications. This paper is in part of an European Program which aims to design a macro cell library for cryptographic applications. (Author abstract) 4 Refs.
Descriptors: *Cryptography; Rapid prototyping; Field programmable gate arrays; Security of data; Parallel algorithms; Pipeline processing systems; Microprocessor chips; Computer hardware description languages
Identifiers: Data encryption standard (DES); Message authentication code (MAC)
Classification Codes:
723.5 (Computer Applications); 723.2 (Data Processing); 722.4 (Digital Computers & Systems)
723 (Computer Software); 716 (Radar, Radio & TV Electronic Equipment); 921 (Applied Mathematics); 722 (Computer Hardware)
72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS); 92 (ENGINEERING MATHEMATICS)

10/5/2 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
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04750506 E.I. No: EIP97073730698
Title: Hardware realization of Krawtchouk transform utilizing VHDL modeling
Author: Botros, N.; Yang, J.; Feinsilver, P.; Schott, R.
Corporate Source: Southern Illinois Univ at Carbondale, Carbondale, IL, USA
Conference Title: Proceedings of the 1997 IEEE Instrumentation & Measurement Technology Conference, IMTC. Part 1 (of 2)
Conference Location: Ottawa, Can Conference Date: 19970519-19970521
Sponsor: IEEE
E.I. Conference No.: 46613
Source: Conference Record - IEEE Instrumentation and Measurement Technology Conference v 1 1997. IEEE, Piscataway, NJ, USA,97CH36022. p 172-177
Publication Year: 1997
CODEN: CRIIE7

Language: English
Document Type: CA; (Conference Article) Treatment: T; (Theoretical)
Journal Announcement: 9709W1
Abstract: In this paper we present a simplification of Krawtchouk transform and its hardware realization on a Xilinx **FPGA** . A brief contrast between this hardware and that of Fourier Transform is presented. The hardware is tested by inputting data through a CAD programs and reading the results of the transform from the RAM of the hardware. These results those calculated by software programs for the same input data. The hardware is stand-alone and operates on a real-time basis. (Author abstract) 8 Refs.
Descriptors: *Signal processing; Fourier transforms; Computer hardware description languages; Computer aided design; Computer aided software engineering; Computer architecture; Random access storage; Computer software; Real time systems; Algorithms
Identifiers: Verilog hardware description languages (**VHDL**); Krawtchouk **transforms** ; Control logic blocks (CLB); Field programmable gate arrays (**FPGA**)
Classification Codes:
723.1.1 (Computer Programming Languages)
716.1 (Information & Communication Theory); 921.3 (Mathematical Transformations); 723.1 (Computer Programming); 723.5 (Computer Applications)
716 (Radar, Radio & TV Electronic Equipment); 921 (Applied Mathematics) ; 723 (Computer Software); 722 (Computer Hardware)
71 (ELECTRONICS & COMMUNICATIONS); 92 (ENGINEERING MATHEMATICS); 72 (COMPUTERS & DATA PROCESSING)

10/5/3 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
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04540673 E.I. No: EIP96100380557
Title: Declarative specification of system independent logic controller programs
Author: Adamski, Marian A.; Monteiro, Joao L.
Corporate Source: Univ of Minho, Minho, Port
Conference Title: Proceedings of the IEEE International Symposium on Industrial Electronics, ISIE'96. Part 1 (of 2)
Conference Location: Warsaw, Poland Conference Date: 19960617-19960620
Sponsor: IEEE; Warsaw University of Technology
E.I. Conference No.: 45484
Source: IEEE International Symposium on Industrial Electronics v 1 1996.,96TH8192. p 305-310
Publication Year: 1996
CODEN: 85PTAR
Language: English
Document Type: CA; (Conference Article) Treatment: T; (Theoretical)
Journal Announcement: 9612W4
Abstract: The relationship between system independent Logic Controller programs (IEC standard 1131-3, Programmable Controllers, Part 3: Programming Languages) and rule-based formal specifications is discussed. The Petri Net and Knowledge Base theories can be joined together in the one context (Gentzen Logic). It combines the advantages taken from mathematical logic with the analysis power of Petri nets. The declarative specification, which is extracted from the description given in the initial standard IEC language (for example from Structured Text), can increase the efficiency of the Logic Controller program development. The well-structured specification, which is represented in the human-readable logic language, has a direct impact on validation, formal verification and implementation of Logic Controller programs. The formality is introduced into design technique, but it also can be used for post-design validations and maintenance. The symbolic deduction technique applied for **PLC** declarative program development appears very attractive. The CAD environment for Application Specific Logic Controllers is a part of research project at University of Minho. The specification in the form of symbolic logic expressions may be verified, and then **transformed** into a format accepted by standard CAD tools (FPLD & **FPGA compilers** , **VHDL** tools). (Author

abstract) 25 Refs.
Descriptors: Computer hardware description languages; Computer software; Knowledge based systems; **Programmable logic controllers** ; Discrete time control systems; Petri nets; Computer aided software engineering; Logic programming
Identifiers: Logic controller programs; Human readable logic language; Symbolic deduction; Discrete event dynamic systems; Mathematical logic
Classification Codes:
723.1.1 (Computer Programming Languages); 723.4.1 (Expert Systems)
723.1 (Computer Programming); 723.4 (Artificial Intelligence); 732.1 (Control Equipment); 731.1 (Control Systems); 921.4 (Combinatorial Mathematics, Includes Graph Theory, Set Theory)
723 (Computer Software); 732 (Control Devices); 731 (Automatic Control Principles); 921 (Applied Mathematics)
72 (COMPUTERS & DATA PROCESSING); 73 (CONTROL ENGINEERING); 92 (ENGINEERING MATHEMATICS)

10/5/4 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
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04403403 E.I. No: EIP96053167730
Title: Rule-based formal specification and implementation of logic controllers programs
Author: Adamski, Marian A.; Monteiro, Joao L.
Corporate Source: Universidade do Minho, Guimaraes, Port
Conference Title: Proceedings of the 1995 IEEE International Aymposium on Industrial Electronics, ISIE'95. Part 2 (of 2)
Conference Location: Athens, Greece Conference Date: 19950710-19950714
Sponsor: IEEE
E.I. Conference No.: 44662
Source: IEEE International Symposium on Industrial Electronics v 2 1995. IEEE, Piscataway, NJ, USA,95TH8081. p 700-705
Publication Year: 1995
CODEN: 85PTAR
Language: English
Document Type: CA; (Conference Article) Treatment: T; (Theoretical)
Journal Announcement: 9607W1
Abstract: The paper describes a proposed framework for the synthesis of structural, rule-based descriptions in Gentzen sequent logic language that could be derived from behavioural descriptions in interpreted Petri net (or Control Petri Net, Grafcet, Sequential Function Chart - SFC, Grafchart formats). The interpreted Petri net is considered as a main, initial specification format for Logic Controller programs. The Gentzen system allows one to naturally simulate and denote the human reasoning and clearly perform symbolic transformations. In such a way it is possible to combine mathematical clarity with practical usefulness. The specification in the form of symbolic expressions may be **transformed** into a format accepted by standard tools (**PLD compilers** , **VHDL** , Logic Controller programming languages) as well as into the standard Boolean expressions. (Author abstract) 22 Refs.
Descriptors: **Programmable logic controllers** ; Knowledge based systems; Formal logic; Petri nets; Computer hardware description languages; Computer simulation; Logic design
Identifiers: Rule based formal specification; Formal design; Grafcet; Sequential function chart; Grafchart; Gentzen sequent logic
Classification Codes:
723.4.1 (Expert Systems); 723.1.1 (Computer Programming Languages)
732.1 (Control Equipment); 723.4 (Artificial Intelligence); 721.1 (Computer Theory, Includes Formal Logic, Automata Theory, Switching Theory, Programming Theory); 921.4 (Combinatorial Mathematics, Includes Graph Theory, Set Theory); 723.1 (Computer Programming); 723.5 (Computer Applications)
732 (Control Devices); 723 (Computer Software); 721 (Computer Circuits & Logic Elements); 921 (Applied Mathematics)
73 (CONTROL ENGINEERING); 72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)

10/5/5 **(Item 5 from file: 8)**
DIALOG(R)File 8:Ei Compendex(R)
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04295712 E.I. No: EIP95122938708
Title: VHDL **and silicon** compiler **experience in the advanced processor interface unit** ASIC **design**
Author: Chang, K.C.; Le, Hugh; Ling, Calvin; Lin, Don
Corporate Source: Boeing Defense and Space Group, Seattle, WA, USA
Conference Title: Proceedings of the 8th Annual IEEE International ASIC Conference and Exhibit
Conference Location: Austin, TX, USA Conference Date: 19950918-19950922
Sponsor: IEEE
E.I. Conference No.: 44005
Source: Proceedings of the Annual IEEE International ASIC Conference and Exhibit 1995. IEEE, Piscataway, NJ, USA,95TH8087. p 329-332
Publication Year: 1995
CODEN: PIAEF2 ISSN: 1063-0988
Language: English
Document Type: CA; (Conference Article) Treatment: A; (Applications); T ; (Theoretical)
Journal Announcement: 9601W4
Abstract: This paper summarizes the process of designing an Advanced Processor Interface Unit (APIU) **ASIC** using **VHDL** simulation, synthesis, and Silicon **Compilation** . Problems and areas for improvements in the interface between different CAD tool environments are addressed. VHDL entity and hierarchy partition guidelines are discussed with examples. (Author abstract)
Descriptors: *Application specific integrated circuits; Integrated circuit layout; Computer simulation; High level languages; Interfaces (computer); Computer aided design; Hierarchical systems; Program compilers; Mathematical models
Identifiers: Advanced processor interface unit; Silicon compilation; Hierarchy partition guidelines; Synopsis design compiler
Classification Codes:
723.1.1 (Computer Programming Languages)
714.2 (Semiconductor Devices & Integrated Circuits); 723.5 (Computer Applications); 723.1 (Computer Programming); 722.2 (Computer Peripheral Equipment); 921.6 (Numerical Methods)
714 (Electronic Components); 723 (Computer Software); 722 (Computer Hardware); 921 (Applied Mathematics)
71 (ELECTRONICS & COMMUNICATIONS); 72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)

10/5/6 **(Item 6 from file: 8)**
DIALOG(R)File 8:Ei Compendex(R)
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04247193 E.I. No: EIP95092850255
Title: Low power ASIC **design for wireless communications**
Author: McGrath, S.; Scully, E.
Corporate Source: Univ of Limerick, Limerick, UK
Conference Title: IEE Electronics Division on Low Power Analogue and Digital VLSI: Asics, Techniques and Applications
Conference Location: London, UK Conference Date: 19950602
E.I. Conference No.: 43523
Source: IEE Colloquium (Digest) n 122 1995. IEE, Stevenage, Engl. p 3/1-3/6
Publication Year: 1995
CODEN: DCILDN ISSN: 0963-3308
Language: English
Document Type: CA; (Conference Article) Treatment: G; (General Review); T; (Theoretical)
Journal Announcement: 9511W1
Abstract: This paper details a design path for the **conversion** of high

level, signal processing blo[redacted]diagrams to **ASIC** design, usi[redacted] **VHDL** . A transceiver module for wireless serial communication between multiple terminals was designed as an **ASIC** using Signal Processing Worksystem (SPW) and Synopsys. Mobile communications systems require compact, low power components to reduce their size and weight. The transceiver connects with passive devices, so it must incorporate control functions to interact smoothly with other devices. SPW was used to design the controller in order to investigate the possibility of **ASIC** design from this level. The high level block diagram was **converted** to **VHDL** using a tool supplied by SPW. To complete the design the code generated by SPW was passed to the Synopsys VLSI design tool, where it is compiled as an **ASIC** . (Author abstract) 5 Refs.

Descriptors: *Application specific integrated circuits; Integrated circuit layout; Radio communication; Computer hardware description languages; Signal processing; Transceivers; Mobile radio systems; Computer aided design; Design aids; VLSI circuits

Identifiers: Software package Signal Processing Worksystem; Software package Synopsys

Classification Codes:

723.1.1 (Computer Programming Languages)

714.2 (Semiconductor Devices & Integrated Circuits); 716.3 (Radio Systems & Equipment); 723.1 (Computer Programming); 716.1 (Information & Communication Theory); 723.5 (Computer Applications)

714 (Electronic Components); 716 (Radar, Radio & TV Electronic Equipment); 723 (Computer Software)

71 (ELECTRONICS & COMMUNICATIONS); 72 (COMPUTERS & DATA PROCESSING)

10/5/7 (Item 7 from file: 8)

DIALOG(R)File 8:Ei Compendex(R)
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03954214 E.I. No: EIP94101417368

Title: Mapping VHDL descriptions of digital systems to FPGAs

Author: Dimond, Keith; Pang, Kam

Corporate Source: Univ of Kent at Canterbury, Canterbury, Engl

Conference Title: Computing and Control Division Colloquium on Software Support and Cad Techniques for FPGAS (Field Programmable Gate Arrays)

Conference Location: London, UK Conference Date: 19940413

Sponsor: Professional Group C2 (Hardware and Systems Engineering)

E.I. Conference No.: 20827

Source: IEE Colloquium (Digest) n 094 Apr 13 1994. Publ by IEE, Michael Faraday House, Stevenage, Engl. p 9/1-9/3

Publication Year: 1994

CODEN: DCILDN ISSN: 0963-3308

Language: English

Document Type: CA; (Conference Article) Treatment: G; (General Review)

Journal Announcement: 9411W3

Abstract: VHDL is the IEEE standard hardware description language. It consists of all the features of a conventional programming language plus additional structures required to represent hardware. These programming structures enable concurrent execution to be defined and mechanisms to describe the assignment of values to signals after delays. The paper describes a method of automating the design route from **VHDL** to **FPGA** . This method employs a **VHDL compiler** to **translate** structural **VHDL** representation into a suitable netlist format and processed by the **FPGA** software to produce the final personality file. The method enables all design decomposition to be carried out in the VHDL environment and thus totally under the control of the designer. 2 Refs.

Descriptors: *Computer aided logic design; Computer hardware description languages; Logic gates; Computer systems; Computer simulation; Computer aided software engineering; High level languages; Program compilers; Data structures; Computer software

Identifiers: Digital systems; **VHDL** ; Field programmable gate arrays; **VHDL compiler** ; Design decomposition

Classification Codes:

723.1.1 (Computer Programming Languages)

721.2 (Logic Elements); 723.1 (Computer Programming); 722.4 (Digital

Computers & Systems); 723.5 (Computer Applications); 723.2 (Data Processing)
721 (Computer Circuits & Logic Elements); 723 (Computer Software); 722 (Computer Hardware)
72 (COMPUTERS & DATA PROCESSING)

10/5/8 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online
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01769415 ORDER NO: AADAA-IMQ47476
Compiling a synchronous programming language into field programmable gate arrays
Author: Shen, Ying
Degree: M.Eng.
Year: 1999
Corporate Source/Institution: Memorial University of Newfoundland (Canada) (0306)
Adviser: Theodore S. Norvell
Source: VOLUME 38/05 of MASTERS ABSTRACTS.
PAGE 1354. 139 PAGES
Descriptors: ENGINEERING, ELECTRONICS AND ELECTRICAL ; COMPUTER SCIENCE
Descriptor Codes: 0544; 0984
ISBN: 0-612-47476-3

This thesis shows how to compile a program expressed by a novel hardware description language, the State Machine Algol-Like Language (SMALL), into Field Programmable Gate Arrays (FPGAs). A “netlist generator” for the SMALL language is created to transform a parallel Algorithmic State Machine (ASM) chart into a structural VHDL description. The one-hot encoding technique is used for the **transformations** . The structural **VHDL** description for the netlist is simulated and synthesised by Synopsys VSS (**VHDL** System Simulator) and Synopsys **FPGA Compiler** , respectively. The netlist is very simple and the components of the netlist consist of only D-type flip-flops and basic gates. The Design Manager of the Xilinx Alliance Series version 1.4 is used to produce configuration data for Xilinx **FPGA** chips. The Xilinx XC4000 family is employed as the target **FPGA** device.

The simulation results for several SMALL programs indicate that the netlist generator performs the specified requirements for all the statements and all the operators in the SMALL language.

Using the netlist generator and existing place-and-route tools makes the implementation of SMALL programs on FPGAs easy. This research offers a significant advance on the original SMALL implementation. Due to its simplicity and simple semantics, it is believed that the SMALL language will be widely used in many areas in the future.

10/5/9 (Item 2 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online
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01767300 ORDER NO: AADAA-I9986271
Compiling SA-C to reconfigurable computing systems
Author: Hammes, Jeffrey Paul
Degree: Ph.D.
Year: 2000
Corporate Source/Institution: Colorado State University (0053)
Adviser: A. P. W. Bohm
Source: VOLUME 61/09-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 4822. 164 PAGES
Descriptors: COMPUTER SCIENCE
Descriptor Codes: 0984
ISBN: 0-599-92604-X

Field Programmable Gate Arrays (FPGAs) have been available for approximately fifteen years and have experienced speed and density

improvements similar to those of microprocessors. Current FPGAs can be reprogrammed in a matter of milliseconds, making them interesting candidates for reconfigurable computing, where specialized circuits can be produced for specific programs to execute more efficiently than a sequential program. Algorithms that are highly regular and exhibit parallelism may benefit from the use of FPGAs.

A significant roadblock to this use of FPGAs is the difficult nature of programming them. Hardware description languages have been the predominant tools for creating **FPGA** circuit configurations, but these languages are low level and require digital circuit expertise as well as explicit handling of timing. To bring FPGAs into mainstream use by conventional programmers, familiar algorithmic language paradigms must be available, with compilers that can convert high level codes to **FPGA** configurations.

This research presents SA-C (derived from “Single-Assignment C”), a pure functional algorithmic language intended for the expression of image processing (IP) applications. SA-C's functional nature makes the compiler's job easier, as compared with imperative languages: parallelism is easy to detect, and analysis and transformations are more straightforward. Perhaps the most important part of the language is its loop <italic>window generators</italic>, which not only express many IP operations in an elegant way but are highly useful in expressing optimizing transformations within the compiler.

A Data Dependence and Control Flow (DDCF) hierarchical graph form is also presented, as an intermediate form with which the SA-C compiler performs its optimizations. These optimizations fall into two broad categories: graph simplifying and loop restructuring. The former are primarily conventional optimizations such as common subexpression elimination and constant folding. The loop restructuring optimizations include loop unrolling, stripmining and fusion, applied as DDCF-to-DDCF transformations using window generators. The compiler, after performing optimizations, is able to convert many inner loops to a low-level, flat dataflow graph designed for **translation** to **VHDL** and finally to **FPGA** configurations. The effects of the **compiler** 's optimizations have been measured on some small kernel codes, and the loop restructuring optimizations are shown to be highly effective.

10/5/10 (Item 1 from file: 65)
DIALOG(R)File 65:Inside Conferences
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04380995 INSIDE CONFERENCE ITEM ID: CN045877565
Systematic Generation of Executing Programs for Processor Elements in Parallel ASIC **or** FPGA **-Based Systems and Their** Transformation **into** VHDL **-Descriptions of Processor Element Control Units**
Maslennikov, O.
CONFERENCE: Parallel processing and applied mathematics-International conference; 4th
LECTURE NOTES IN COMPUTER SCIENCE, 2002; (NO) 2328 P: 272-279
Berlin, London, Springer, 2002
ISSN: 0302-9743 ISBN: 3540437924
LANGUAGE: English DOCUMENT TYPE: Conference Revised papers
CONFERENCE EDITOR(S): Wyrzykowski, R.
CONFERENCE LOCATION: Naleczow, Poland 2001; Sep (200109) (200109)

BRITISH LIBRARY ITEM LOCATION: 5180.185000
NOTE:
Includes bibliographical references and index
DESCRIPTORS: parallel processing; applied mathematics; PPAM

10/5/11 (Item 2 from file: 65)
DIALOG(R)File 65:Inside Conferences
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01008752 INSIDE CONFERENCE ITEM ID: CN009862160
VLSI Design of a Custom ASIC **Using** VHDL **for** Converting **12-Bit Binary**

to BCD
Guy, B. M.
CONFERENCE: System theory-27th Southeastern symposium
SOUTHEASTERN SYMPOSIUM ON SYSTEM THEORY, 1995; VOL 27 P: 409-413
IEEE Computer Society Press, 1995
ISSN: 0094-2898 ISBN: 0818669853
LANGUAGE: English DOCUMENT TYPE: Conference Papers
CONFERENCE SPONSOR: IEEE
CONFERENCE LOCATION: Starkville, MS
CONFERENCE DATE: Mar 1995 (199503) (199503)

BRITISH LIBRARY ITEM LOCATION: 8352.497000
NOTE:
Also known as 27th SSST
DESCRIPTORS: system theory; SSST; IEEE

10/5/12 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC
(c) 2003 Institution of Electrical Engineers. All rts. reserv.

7479562 INSPEC Abstract Number: B2003-01-1265B-103, C2003-01-5210B-080
Title: Dynamic hardware plugins (DHPs) in an FPGA with partial run-time reconfiguration (RTR)
Author(s): Horta, E.L.; Lockwood, J.W.; Taylor, D.E.; Parlour, D.
Author Affiliation: Washington Univ., St. Louis, MO, USA
Conference Title: FPGA 2002. Tenth ACM International Symposium on Field-Programmable Gate Arrays p.250
Publisher: ACM, New York, NY, USA
Publication Date: 2002 Country of Publication: USA viii+258 pp.
ISBN: 1 58113 452 5 Material Identity Number: XX-2002-00779
U.S. Copyright Clearance Center Code: 1-58113-452-5/02/0002...$5.00
Conference Title: Proceedings of FPGA'02: ACM/SIGDA International Symposium on Field Programmable Gate Arrays
Conference Sponsor: ACM
Conference Date: 24-26 Feb. 2002 Conference Location: Monterey, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Applications (A); Practical (P)
Abstract: Summary form only given. A practical system for RTR of networked hardware has been developed that includes PARBIT (a configuration bitfile manipulation program), a gasket interface that interconnects blocks of logic, as well as the design rules to make partial RTR feasible. The Reconfigurable Applications Device (RAD), an XCV2000E present in the Washington University Field-Programmable Port Extender (FPX), performs packet processing functions on data flowing into and out of a network. The RAD is logically partitioned into several identical DHP sites surrounded by a static infrastructure which provides access to off-chip memory, the data ports of the network switch, and interconnection between DHP sites. Application developers are given a DHP interface definition and tool suite which can be used to **compile** any conforming **VHDL** module into a partial **FPGA** bitfile. This bitfile can then be downloaded into any DHP site using partial reconfiguration without disturbing the operation of the infrastructure or other DHP sites.
Subfile: B C
Descriptors: field programmable gate arrays; hardware description languages; logic CAD; reconfigurable architectures
Identifiers: dynamic hardware plugins; **FPGA** ; partial run-time reconfiguration; RTR; networked hardware; PARBIT; configuration bitfile manipulation program; gasket interface; design rules; Reconfigurable Applications Device; XCV2000E; Washington University Field-Programmable Port Extender; packet processing functions; static infrastructure; off-chip memory; VHDL
Class Codes: B1265B (Logic circuits); B1265A (Digital circuit design, modelling and testing); B1130B (Computer-aided circuit analysis and design) ; C5210B (Computer-aided logic design); C7410D (Electronic engineering computing); C6110F (Formal methods); C5120 (Logic and switching circuits)
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10/5/13 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC
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7479286 INSPEC Abstract Number: C2003-01-5210-026
Title: Hardware Petri nets on programmable devices
Author(s): Nakamura, M.; Amau, Y.; Matsumura, T.; Nagayama, I.; Yamashiro, T.
Author Affiliation: Ryukyus Univ., Okinawa, Japan
Journal: Transactions of the Institute of Electrical Engineers of Japan, Part C vol.122-C, no.7 p.1202-8
Publisher: Inst. Electr. Eng. Japan,
Publication Date: July 2002 Country of Publication: Japan
CODEN: DGRCDZ ISSN: 0385-4221
SICI: 0385-4221(200207)122C:7L.1202:HPNP;1-I
Material Identity Number: T197-2002-009
Language: Japanese Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: Petri nets are a mathematical tool well suited for modeling and analysis of Discrete Event Dynamic Systems (DEDS). In this paper, we propose and implement hardware Petri nets on programmable devices. The hardware Petri nets are generated by firstly modeling the target system with a GUI tool, secondly **converting** the net description into **VHDL** codes and finally implementing onto **FPGA** devices. The hardware Petri nets are useful for discrete event simulation in which they can represent perfectly the natural parallelism of the target system at the circuit level. Moreover, our proposed system is regarded as a logic circuit development system in which we can design desired logic circuits by using Petri nets and implement them directly on FPGAs. (19 Refs)
Subfile: C
Descriptors: discrete event simulation; field programmable gate arrays; graphical user interfaces; hardware description languages; logic design; Petri nets
Identifiers: hardware Petri nets; programmable devices; discrete event dynamic systems; GUI tool; VHDL codes; **FPGA** devices; discrete event simulation; target system parallelism; logic circuit development systems; logic circuit design
Class Codes: C5210 (Logic design methods); C1160 (Combinatorial mathematics); C5120 (Logic and switching circuits); C6180G (Graphical user interfaces); C6185 (Simulation techniques)
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10/5/14 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC
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7462525 INSPEC Abstract Number: B2003-01-6210R-010
Title: FPGA implementation of the wavelet packet transform for high speed communications
Author(s): Jamin, A.; Mahonen, P.
Author Affiliation: Center for Wireless Commun., Oulu Univ., Finland
Conference Title: Field-Programmable Logic and Applications. Reconfigurable Computing Is Going Mainstream. 12th International Conference, FPL 2002. Proceedings (Lecture Notes in Computer Science Vol.2438) p.212-21
Editor(s): Glesner, M.; Zipf, P.; Renovell, M.
Publisher: Springer-Verlag, Berlin, Germany
Publication Date: 2002 Country of Publication: Germany xxii+1187 pp.
ISBN: 3 540 44108 5 Material Identity Number: XX-2002-02825
Conference Title: Field-Programmable Logic and Applications. Reconfigurable Computing Is Going Mainstream. 12th International Conference, FPL 2002. Proceedings
Conference Date: 2-4 Sept. 2002 Conference Location: Montpellier, France
Language: English Document Type: Conference Paper (PA)

Treatment: Applications (A); Practical (P); Theoretical (T)
Abstract: Recent work has shown interest in wavelet-packet based modulation (WPM). This scheme is implemented with an architecture similar to orthogonal frequency division multiplex (OFDM), except for using the wavelet packet transform (WPT) in place of the Fourier transform. In this article, we study the implementation complexity of a WPT suitable for such a modulation scheme. A speed optimized implementation of the Mallat algorithm based on a generic reconfigurable filter structure is proposed. Measured complexity results of the designed **transform** implemented in **FPGA** using **VHDL** are reported and commented. (4 Refs)
Subfile: B
Descriptors: field programmable gate arrays; FIR filters; hardware description languages; multimedia communication; OFDM modulation; transceivers; wavelet transforms
Identifiers: **FPGA** implementation; wavelet packet transform; high speed communications; wavelet-packet based modulation; orthogonal frequency division multiplex; implementation complexity; Mallat algorithm; generic reconfigurable filter; VHDL
Class Codes: B6210R (Multimedia communications); B0290X (Integral transforms in numerical analysis); B6120 (Modulation and coding methods); B6150C (Communication switching); B1270F (Digital filters)
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10/5/15 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC
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6470821 INSPEC Abstract Number: B2000-02-6120D-055, C2000-02-5140-003
Title: Hardware implementation of cryptographic systems
Author(s): Heinig, A.
Journal: Elektronik vol.48, no.23 p.70-2, 74
Publisher: WEKA-Fachzeitschriften,
Publication Date: 16 Nov. 1999 Country of Publication: Germany
CODEN: EKRKAR ISSN: 0013-5658
SICI: 0013-5658(19991116)48:23L.70:HICS;1-H
Material Identity Number: E071-1999-024
Language: German Document Type: Journal Paper (JP)
Treatment: Applications (A); Practical (P); Experimental (X)
Abstract: Deals with cryptographic public key systems using several ASICs. Compares hardware and software solutions and describes briefly the RSA (Rivest, Shamir and Adleman) public-key encoding systems. Encryption security is discussed and it is noted that the hardware solution can be relatively fast. The system was designed in the **VHDL** language and **converted** to code for **ASIC** implementation. (4 Refs)
Subfile: B C
Descriptors: application specific integrated circuits; firmware; hardware description languages; public key cryptography
Identifiers: cryptographic systems; public key systems; ASICs; RSA; encoding systems; hardware solution; VHDL language
Class Codes: B6120D (Cryptography); C5140 (Firmware); C6130S (Data security)
Copyright 2000, IEE

10/5/16 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC
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6154771 INSPEC Abstract Number: C1999-03-5210B-038
Title: JVX-a rapid prototyping system based on Java and FPGAs
Author(s): Macketanz, R.; Karl, W.
Author Affiliation: Inst. fur Inf., Tech. Univ. Munchen, Germany
Conference Title: Field-Programmable Logic and Applications. From FPGAs to Computing Paradigm. 8th International Workshop, FPL'98. Proceedings p.99-108
Editor(s): Hartenstein, R.W.; Keevallik, A.
Publisher: Springer-Verlag, Berlin, Germany

Publication Date: 1998 Country of Publication: Germany xi+533 pp.
ISBN: 3 540 64948 4 Material Identity Number: XX-1998-02499
Conference Title: Field-Programmable Logic and Applications. From FPGAs to Computing Paradigm. 8th International Workshop, FPL '98. Proceedings
Conference Date: 31 Aug.-3 Sept. 1998 Conference Location: Tallinn, Estonia
Language: English Document Type: Conference Paper (PA)
Treatment: Applications (A); Practical (P)
Abstract: The paper describes the JVX system which combines hardware/software codesign aspects with rapid prototyping techniques. Applications for embedded systems written in Java are **translated** into a **VHDL** description. The hardware platform of the JVX system consists of **FPGA** facilitating the execution of the synthesized **VHDL** code, and the communication with the interpreted Java byte code via a PCI interface. The JVX system enables the generated hardware parts and corresponding Java byte code of an application to be mutually exchanged allowing the developer to find a good tradeoff between the hardware costs and performance requirements. (21 Refs)
Subfile: C
Descriptors: embedded systems; field programmable gate arrays; hardware description languages; hardware-software codesign; Java; software prototyping
Identifiers: rapid prototyping system; **FPGA** ; JVX system; hardware/software codesign; embedded systems; synthesized VHDL code; interpreted Java byte code; PCI interface; hardware costs; performance requirements
Class Codes: C5210B (Computer-aided logic design); C5215 (Hardware-software codesign); C7410D (Electronic engineering computing)
Copyright 1999, IEE

10/5/17 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC
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5148105 INSPEC Abstract Number: B9602-1265B-037, C9602-5210B-056
Title: Personal computer circuit synthesis tools for FPGAs
Author(s): Huber, J.
Author Affiliation: Mentor Graphics, Munchen, Germany
Journal: Elektronik Industrie vol.26, no.6 p.68
Publisher: Huthig,
Publication Date: June 1995 Country of Publication: West Germany
CODEN: EKIDAT ISSN: 0374-3144
SICI: 0374-3144(199506)26:6L.68:PCCS;1-A
Material Identity Number: E175-95007
Language: German Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: The author discusses applications of various logic circuit design tools using the VHDL language, and investigates circuit simulation methods. Practical **conversion** of a **VHDL** design file into a **FPGA** (field **programmable gate array**) device, using the ACTEL program is described. A training course in the use of the design tool is available as a CD-ROM. (0 Refs)
Subfile: B C
Descriptors: field programmable gate arrays; hardware description languages; logic CAD; microcomputer applications
Identifiers: personal computer circuit synthesis tools; logic circuit design tools; VHDL; circuit simulation methods; **FPGA** ; ACTEL program; training course; CD-ROM
Class Codes: B1265B (Logic circuits); B1130B (Computer-aided circuit analysis and design); C5210B (Computer-aided logic design); C7410D (Electronic engineering computing); C5120 (Logic and switching circuits); C6140D (High level languages)
Copyright 1996, IEE

10/5/18 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

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03405097 INSPEC Abstract Number: C89042638
Title: Integrated Design Automation System (IDAS)
Journal: SIGMICRO Newsletter vol.19, no.4-vol.20, no.1 p.11-17
Publication Date: March 1989 Country of Publication: USA
CODEN: SIGMDJ ISSN: 0163-5751
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P); Product Review (R)
Abstract: The Integrated Design Automation System (IDAS) is designed to assist users in solving embedded computer design and application problems. Towards this end, the IDAS provides: rapid prototyping tools; rapid design tradeoff (hardware and software) facilities; and rapid measurement of design quality and detection of design weaknesses. Major features of the system include: ADA to Microcode **compilation** ; **VHDL** driven automatic retargeting; Ada to **VHDL** synthesis; Ada to **ASIC** chips synthesis; design process instrumentation; and Ada support stylized automatically for each target machine. The JRS IDAS is implemented on a DEC VAX and IBM PCs. (0 Refs)
Subfile: C
Descriptors: development systems; software tools
Identifiers: Integrated Design Automation System; embedded computer design; rapid prototyping tools; rapid design tradeoff; rapid measurement; design quality; ADA to Microcode compilation; VHDL driven automatic retargeting; Ada to VHDL synthesis; Ada to **ASIC** chips synthesis; design process instrumentation; JRS IDAS
Class Codes: C5250 (Microcomputer techniques); C6115 (Programming support); C7410D (Electronic engineering); C7430 (Computer engineering)

10/5/19 (Item 1 from file: 111)
DIALOG(R)File 111:TGG Natl.Newspaper Index(SM)
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04923229 Supplier Number: 18572971
FPGA **Synthesis Leader Offers VHDL Discovery Kit Based on Its Popular Galileo Design Environment; PC-based Kit Targets** FPGA **Designers** Converting **From Schematics to** VHDL **-based Design, Offers Migration Path to Exemplar's Galileo and Leonardo Design Environments.**
Business Wire, p8120302
August 12, 1996
LANGUAGE: English RECORD TYPE: Citation

COMPANY NAMES: Exemplar Logic Inc.--Product introduction
DESCRIPTORS: Computer software industry--Product introduction
PRODUCT NAMES: 7372510 (Computer Language Software ex Military)
SIC CODES: 7372 Prepackaged software
FILE SEGMENT: NW File 649

10/5/20 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS
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2204161 NTIS Accession Number: ADA391952/XAB
Low Power Application-Specific Integrated Circuit (ASIC) implementation of Wavelet Transform/Inverse Transform
(Master's thesis)
Harvala, D. N.
Air Force Inst. of Tech., Wright-Patterson AFB, OH. School of Engineering.
Corp. Source Codes: 000805002; 012225
Report No.: AFIT/GE/ENG/01M-14
Mar 2001 132p
Languages: English Document Type: Thesis
Journal Announcement: USGRDR0123
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fax at (703)605-6900; and email at orders@ntis.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A08/MF A02
Country of Publication: United States
A unique **ASIC** was designed implementing the Haar Wavelet transform for image compression/decompression. **ASIC** operations include performing the Haar wavelet transform on a 512 by 512 square pixel image, preparing the image for transmission by quantizing and thresholding the transformed data, and performing the inverse Haar wavelet transform, returning the original image with only minor degradation. The **ASIC** is based on an existing four-chip **FPGA** implementation. Implementing the design using a dedicated **ASIC** enhances the speed, decreases chip count to a single die, and uses significantly less power compared to the **FPGA** implementation. A reduction of RAM accesses was realized and a tradeoff between states and duplication of components for parallel operation were key to the performance gains. Almost half of the external RAM accesses were removed from the **FPGA** design by incorporating an internal register file. This reduction reduced the number of states needed to process an image increasing the image frame rate by 13% and decreased I/O traffic on the bus by 47%. Adding control lines to the ALU components, thus eliminating unnecessary switching of combination logic blocks, further reduced power requirements. The 22 mm2 **ASIC** consumes an estimated 430 mW of power when operating at the maximum frequency of 17 MHz.
Descriptors: *Wavelet transforms; *Image compression; Theses; Gates(Circuits); Integrated circuits
Identifiers: Vlsi; Haar wavelet **transform** ; Haar wavelet inverse **transform** ; **Fpga** (Field programmable gate arrays); **Vhdl** (**Very high speed integrated circuit description** language); **Asic** (Application specific integrated circuits); NTISDODXA
Section Headings: 49GE (Electrotechnology--General); 62GE (Computers, Control, and Information Theory--General)

10/5/21 (Item 2 from file: 6)
DIALOG(R)File 6:NTIS
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1962826 NTIS Accession Number: TIB/A96-03346
JESSI AC-8: synthesis, optimization and analysis. Final report
Langmaier, A.
Siemens A.G., Erlangen (Germany, F.R.).
Corp. Source Codes: 056225000; 5719500
6 Jul 95 51p
Languages: English
Journal Announcement: GRAI9619
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC E09
Country of Publication: Germany, Federal Republic of
Contract No.: BMBF 01M2869A
New tools with extended functionality are described for supported design of ASICs and systems covering all areas of synthesis from architecture synthesis to logic and layout synthesis: The high-level synthesis tool Callas could be improved and finished. Functionality demonstration includes design of an ATM switching node for an **ASIC** . VOTAN offers high-level **VHDL** code **transformations** which reduce the effort to write VHDL code by providing a more general description style and optimize the code with respect to the RT-level synthesis step. TOS supports the most important **FPGA** technology (e.g. Xilinx, Altera). The Micro-controller Interface Generator MIG increases the productivity of a hardware designer, and the Circuit Verification Environment CVE supports the formal analysis and verification of digital circuits. SIDECON is a knowledge based design system that produces a PCB design using standard components. The tool ECTP combines timing and area optimization technique. Strategies of tool marketing and further development are outlined. (WEN). (Copyright (c) 1996 by FIZ. Citation no. 96:003346.)

Descriptors: *Control dom[illegible]ted application; *Microcontrol[illegible] interface; *Register transfer level synthesis; *Electronic systems design; System-level design; Integrated circuits; Boolean functions; Expert systems ; High-level synthesis system
Identifiers: *Foreign technology; NTISTFFIZ
Section Headings: 62C (Computers, Control, and Information Theory--Control Systems and Control Theory)

10/5/22 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal
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14686107 PASCAL No.: 00-0360815
Interfacing compiled fpga **programs : the MMAlpha approach**
Interfacage de programmes compiles pour FPGA **: l'approche dans MMAlpha**
DERRIEN Steven; RISSET Tanguy
CNRS. Institut de recherche en informatique et systemes aleatoires, Rennes, France; Universite de Rennes 1. Institut de recherche en informatique et systemes aleatoires, Rennes, France; Institut national des sciences appliquees de Rennes. Institut de recherche en informatique et systemes aleatoires, Rennes, France; Institut national de recherche en informatique et en automatique. Institut de recherche en informatique et systemes aleatoires, Rennes, France
Journal: Publication interne - IRISA, 2000 (1331) 11 p., fig. Non-paginated pages/foldouts
ISSN: 1166-8687 Availability: INIST-22588; 354000085200420000
No. of Refs.: 16 ref.
Report No.: IRISA-PI 200-1331
Document Type: P (Serial); R (Report) ; M (Monographic)
Country of Publication: France
Language: English Summary Language: English; French
Le processus de **compilation** pour un coprocesseur **FPGA** doit produire un programme **VHDL** qui sera, a son tour, **compile** par des outils commerciaux en une configuration qui sera chargee sur le **FPGA** . Pour etre complet, l'architecture concue doit etre interfacee avec le processeur hote. Nous decrivons les technique employees pour generer une interface efficace pour les programmes VHDL generes par l'outil MMAlpha : des reseaux systoliques lineaires. Plus precisement, nous montrons comment concevoir une interface parametree qui sera generique et automatiquement generee pour chaque reseau systolique concu. Nous presentons aussi des resultats experimentaux de l'implementation de telles interfaces sur des carte acceleratrices a base de **FPGA** .

English Descriptors: Circuit design; VLSI circuit; Field **programmable gate array** ; Systolic network; High level synthesis; Compiler; Co-design

French Descriptors: Conception circuit; Circuit VLSI; Reseau porte programmable; Reseau systolique; Synthese haut niveau; Compilateur; conception conjointe

Classification Codes: 430A09H; 001D03F06A

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10/5/23 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal
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12551311 PASCAL No.: 96-0231644
Conception en vue d'une realisation d'un systeme de vision tridimensionnel
(Conception and realization of a 30 vision system)
MERIBOUT Mahmoud; HOU KUN MEAN, dir
Universite de Compiegne, Compiegne, Francee

Univ.: Universite de Compiegne. Compiegne. FRA Degree: Th. doct.
1995-01; 1995 129 p.
Availability: INIST-T 102476; T95COMP776S
No. of Refs.: 61 ref.
Document Type: T (Thesis) ; M (Monographic)
Country of Publication: France
Language: French Summary Language: French; English

Le developpement de la technologie VLSI a considerablement ameliore la puissance de calcul des machines inintelligentes, permettant le traitement des applications complexes avec un faible cout. Neanmoins, malgre les grands succes connus dans beaucoup de domaines, les problemes de vision sont souvent mal definis, mal poses ou consomment un temps de calcul non negligeable. Ceci a pour effet de contraindre les concepteurs de limiter le domaine d'application: solution pouvant etre inefficace dans le cas ou de nouveaux algorithmes plus performants apparaissent. Le but des travaux presentes dans le cadre de these consiste a etudier et a mettre en oeuvre un systeme de perception realisant plusieurs algorithmes de vision, tels que la detection des contours et l'estimation de mouvements en temps reel, compression-decompression rapide des images, etc La robustesse de notre systeme de vision reside en sa flexibilite, sa reconfigurabilite, son extensibilite, et sa modularite. Le principe de conception de notre architecture est base selon les besoins en termes de communication, de puissance de calcul, de flux de donnees d'entrees et de stockage pour chacun des trois niveaux de traitement. A cet effet, un bus image materiel a ete mis au point reliant toutes les sources possibles d'images que sont: - Un module d'acquisition et de compression-decompression video en norme JPEG, - Un module de traitement bas niveau temps reel, reconfigurable dynamiquement et realisant des operateurs de traitement d'images cables, en telechargeant les programmes **compiles** en **VHDL** sur le composant **FPGA** , - Un module de traitement haut niveau et niveau intermediaire base sur le TMS320c40. L'avantage de notre architecture est sa reconfigurabilite pour les trois niveaux de traitement: Un module a base de composants **FPGA** pour le traitement bas niveau, et un reseau d'interconnexion dynamiquement reconfigurable pour le traitement haut niveau et niveau intermediaire. Ceci nous permet de considerer notre system

English Descriptors: Circuit synthesis; Description language; Multiprocessor; Artificial vision; Computer vision; Real time system; VLSI circuit; Image processing; Circuit architecture; Field **programmable gate array**

French Descriptors: Synthese circuit; Langage description; Multiprocesseur; Vision artificielle; Vision ordinateur; Systeme temps reel; Circuit VLSI; Traitement image; VHDL; Bus image; Filtre Deriche; Operateur cable; Architecture circuit; Reseau porteprogrammable

Classification Codes: 001D03F06B

10/5/24 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
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01304851 Genuine Article#: GM880 Number of References: 0
Title: VHDL PLD COMPILER **FOR STATE-MACHINES**
Author(s): TUCK B
Journal: COMPUTER DESIGN, 1991, V30, N14, P135
Language: ENGLISH Document Type: ARTICLE
Subfile: SciSearch
Journal Subject Category: COMPUTER APPLICATIONS & CYBERNETICS; ENGINEERING, ELECTRICAL & ELECTRONIC

10/5/25 (Item 1 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs
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1127630 H.W. WILSON RECORD NUMBER: BAST93059794

First-time users must understand the productivity gains offered by the tools, not the language

Ganousis, Dan;

Computer Design v. 32 (Oct. '93) p. A18+
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ABSTRACT: Part of a supplement on the design of application-specific integrated circuits (ASICs). The writer describes the virtues of VHDL compared to Verilog hardware description language (HDL) for the first-time user. HDLs are modeling languages and not simulators. The function of Verilog HDL, whether that of a language, a simulator, or both is not clear. VHDL, on the other hand, is a language and not a simulator, although implementing the System-1076 **VHDL compiler** on the front end of Mentor's QuickSim II **ASIC** simulator has given designers a complete simulation environment from **VHDL** to gate-level sign-off, all within a single simulation environment with a single **ASIC** library. Furthermore, VHDL has sufficient and available libraries, although Verilog vendors tout the number of libraries available as a key advantage over VHDL. A complementary article in the supplement highlights the benefits of Verilog HDL over VHDL.

DESCRIPTORS: VHDL (Computer hardware description language); EDA software;